JOURNAL OF MATERIALS SCIENCE **34** (1999) 3375–3396

The AC electrical characterization of the solid-state reaction derived $CaSnO_3$

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The potential of $CaSnO_3$ (calcium metastannate) for its application as a capacitor component possessing small temperature coefficient of capacitance (TCC) in electrical systems, is examined via the ac small-signal measurements. The ac electrical data were acquired on these samples sintered at various combinations of temperature-time frames ($1200\,^{\circ}C \leq T \leq 1350\,^{\circ}C$; $24\ h \leq t \leq 60\ h$) in the frequency range from 5 Hz to 13 MHz. The measurements were carried out over the temperature range 25–300 °C. The electrical response was found to exhibit relaxation processes in more than one complex plane formalism in a simultaneous fashion. The resistance of the sintered samples was dominated by the grain boundaries. The capacitance showed almost linear behavior in this measurement temperature range. The resulting electrical behavior has been discussed with the evolved microstructure in the sintered bodies.

1. Introduction

The perovskite-structured compounds in the MO-SnO_2 (M = Ca, Sr and Ba) system representing $MSnO_3$, have been projected as novel electroceramics, due to potential applications in pure as well as in doped modification, as gas sensors and capacitor components in high speed electronic devices [1–3]. For use in the RC (resistor-capacitor) or LC (inductor-capacitor) circuits, the temperature coefficient of capacitance (TCC) becomes important as high dielectric loss results in the generation of heat. This heat generation causes to increase the temperature of the capacitor. In such applications, the required level of variation with temperature should either be zero (which is ideal), or a small reproducible value that compensates for a variation in the rest of the circuit [4].

A vigorous and systematic investigation on the synthesis, processing and microstructural aspects of $MSnO_3$ systems has recently been reported in the literature [5–7]. In order to exploit these materials as gas sensing devices and/or capacitor components, possessing the above mentioned temperature independent characteristics, it is imperative that the electrical conduction and the effect of surface and bulk morphologies in these materials be well understood, so that the processing parameters can be optimized. Since these devices are made mostly from the polycrystalline materials, it is also important to understand the sequential contributions of grain, grain boundaries and other phases including physically distinct regions in the microstructure. Thus, a correlation among the processing, microstructure and resulting electrical behavior of these materials is warranted. Such a correlation is not adequately addressed in the recent literature [8–10], wherein the variation of capacitance and dielectric loss in the temperature range of 27 to 227 °C at three spot frequencies (1, 10 and 100 kHz) only have been reported. Moreover, the samples used in these studies were sintered at a single temperature for one soak-time, and therefore, the results obtained are not likely to be representative of the true behavior of the material investigated.

In this work, the ac small-signal response of dense $CaSnO_3$ ceramic bodies, sintered at various temperature and soak-time profiles, in the frequency (f) domain (5 Hz through 13 MHz) has been evaluated over the temperature range 25 through 300 °C. The objective is to assess the magnitude of temperature dependence of the capacitance of these ceramics. The ac small-signal electrical data were analyzed via lumped parameter/complex plane analysis (LP/CPA) technique to unravel the underlying competing phenomena attributing to the complexity of the microstructure. This approach is well known as the immittance (impedance/admittance) spectroscopy (IS). The LP/CPA technique has proven to be a useful means of characterizing the electrical nature of a number of polycrystalline heterogeneous materials and devices [11–16, 19]. An application of such a technique reveals the degree of structural uniformity, variation in electrical

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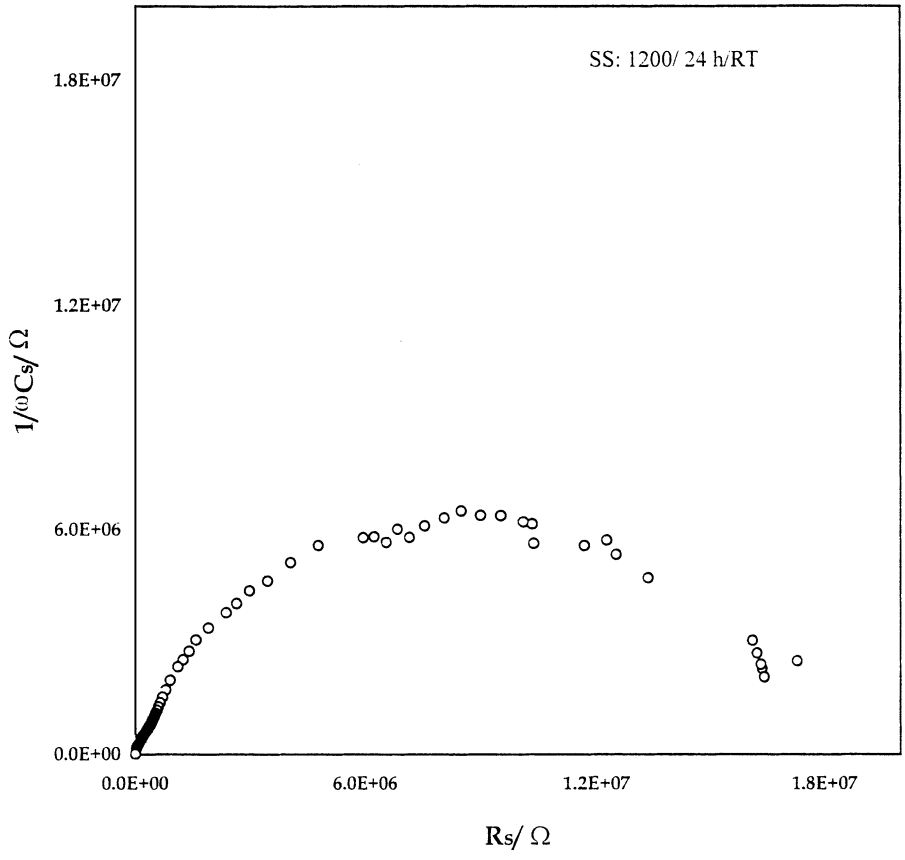
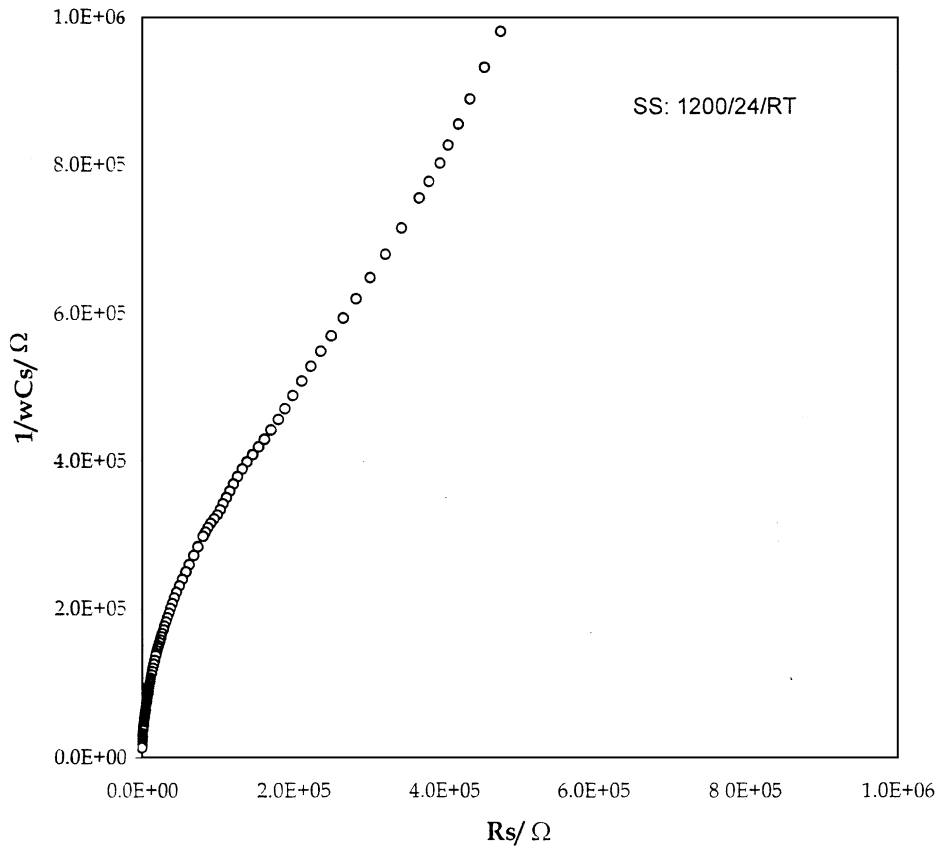
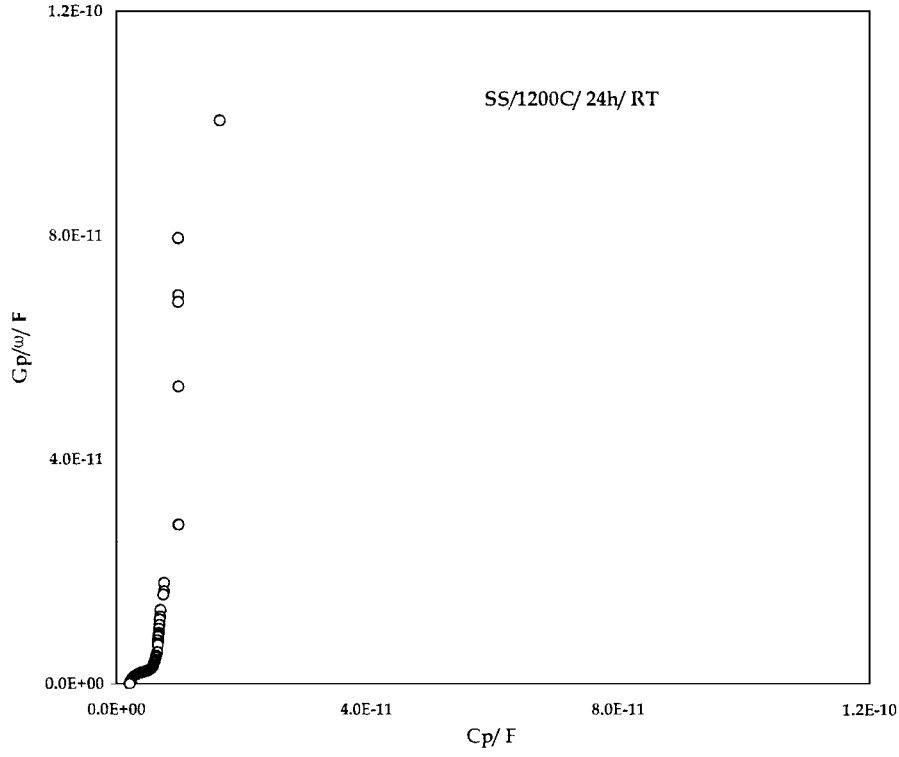


(a)



(b)

Figure 1 Room temperature complex plane plots for $CaSnO_3$ samples synthesized via solid-state reaction and sintered at 1200 °C for 24 h. (a) Impedance (Z^*) plot; (b) exploded view of the impedance (Z^*) plot at high frequencies; (c) complex capacitance (C^*) plot of the same data as in (a); (d) exploded view of the C^*-plane plot at high frequencies; (e) modulus (M^*) plot representation of the same data as in (a). (*Continued*).



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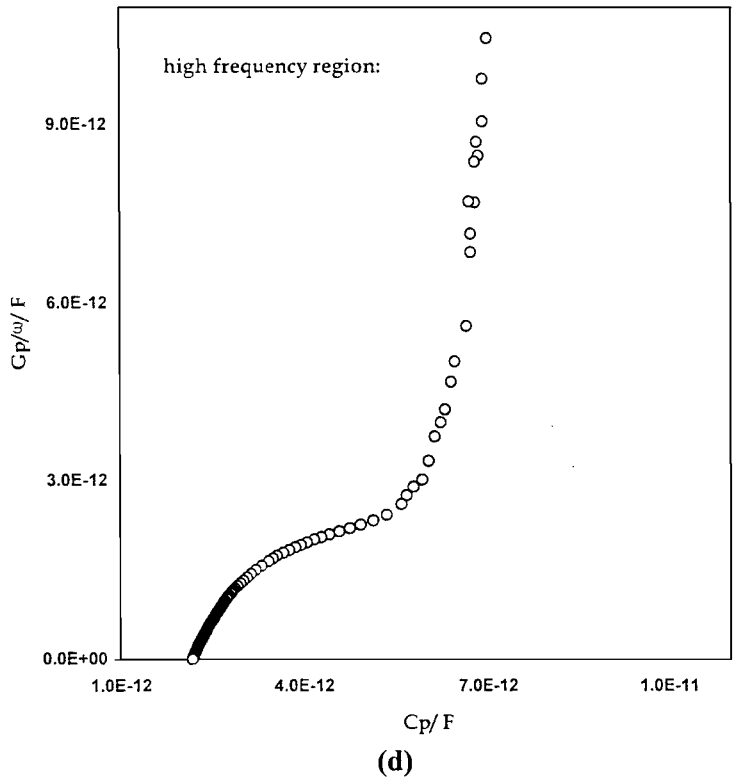

(d)

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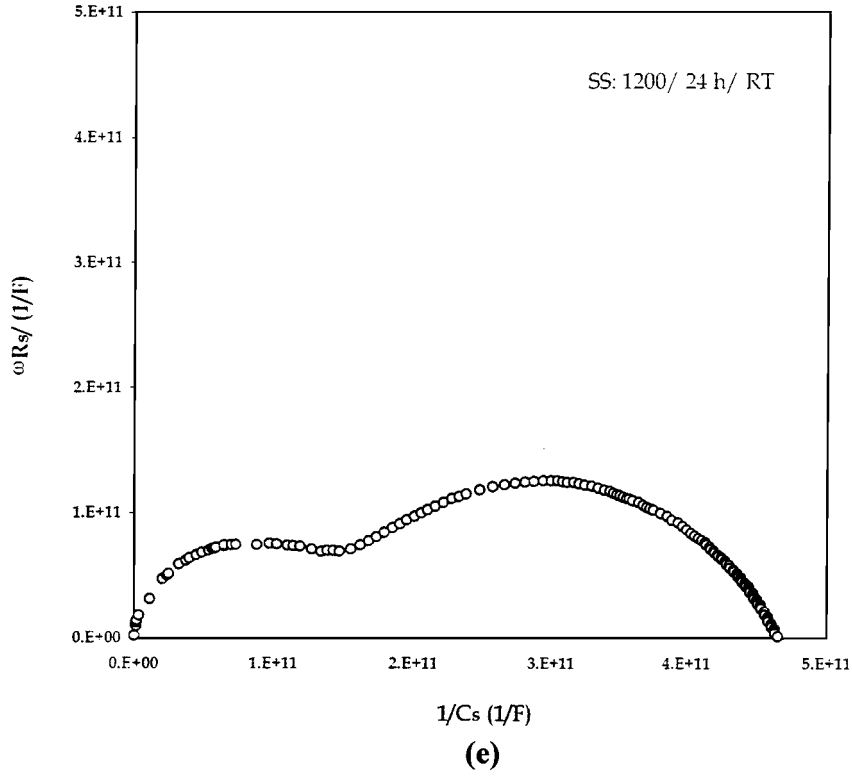
conduction path, stability, degradation, time-dependent processes, etc. in such materials or device systems.

2. Experimental

2.1. Solid-state reaction route and sample preparation

The samples investigated in this work were synthesized via the traditional solid-state reaction (SSR), the details of which have been reported elsewhere [6] and are briefly mentioned in the following subsection. Beside this, novel methods such as, self-heat-sustained (SHS), sol-gel and organometallic (citrate precursor) complex techniques were also employed for sample synthesis. It should be pointed out that the idea of adopting various synthesis processes was two-fold: first, the limited amount of literature available on this material employed SSR route which is presumed to be a conventional



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method. Second, it was intended to find a favorable synthesis technique in terms of the phase purity and benign microstructure in the sintered samples with desired electrical characteristics. The electrical behavior of the SHS-derived $CaSnO_3$ samples have been recently reported [17].

2.1.1. Solid-state reaction route

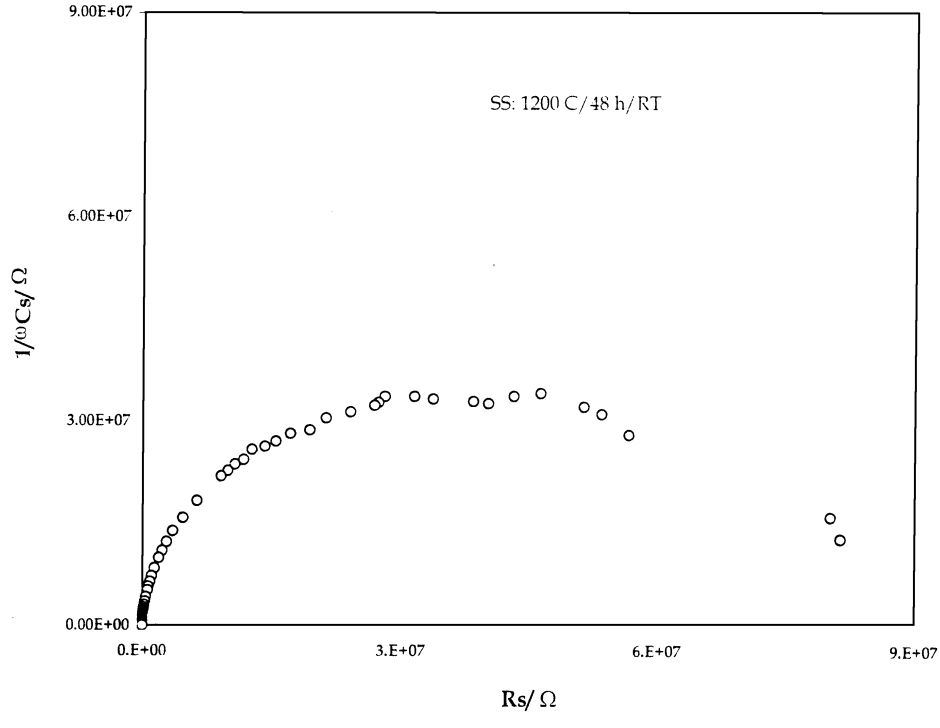
Equimolar (1 : 1) amounts of the compound $Ca(NO_3)_2 \cdot 4H_2O$ and SnO_2 powder were dry mixed in an agate mortar. The mixture was then ball-milled for 8 h in isopropyl alcohol medium. Subsequently, the powder was dried in an air oven overnight, pressed uniaxially into discs 6 or 12 mm in diameter and 2–3 mm in thickness using stainless steel die at a pressure of 100 MPa. The mixture was calcined in air at 1000 °C for 24 h. The pellets were crushed and ground to a fine homogeneous powder which was subjected to phase analysis by powder X-ray diffraction to confirm the formation of $CaSnO_3$ as a single phase. The resulting XRD pattern was also used to detect the presence of, if any, unreacted starting materials and/or new Ca or Sn-rich phases.

The calcined powder was subjected to sintering (in order to follow the evolution of microstructure and its effect on the measured electrical properties) at two different temperatures, viz. at 1200 and 1350 °C, for duration ranging from 24 to 60 h in ambient air. Prior to sintering, the calcined powder was blended with 10 wt % polyvinyl alcohol as binder, dried under UV lamp and pressed into green pellets by uniaxial pressing at pressures not exceeding 100 MPa. The use of polyfunctional organics such as polyvinyl alcohol (PVA) or polyethylene glycol (PEG) is a common practice in the sintering of ceramic bodies, which plays an important role in the microstructural development. The organic binders are believed to provide strength and lubrication effect thereby bringing the particles in the green body closer to one another. This assists in achieving higher densities in sintered bodies than those sintered without the binder. The choice of PVA in this work was due to its relatively easier combustion kinetics compared to those of PEG. The choice of a rather wide temperature-time (T-t) schedule in this work was due to the fact that the single report available in the literature on $CaSnO_3$, indicated only one sintering step (1350 °C/12 h in air) [8] without any microstructural features.

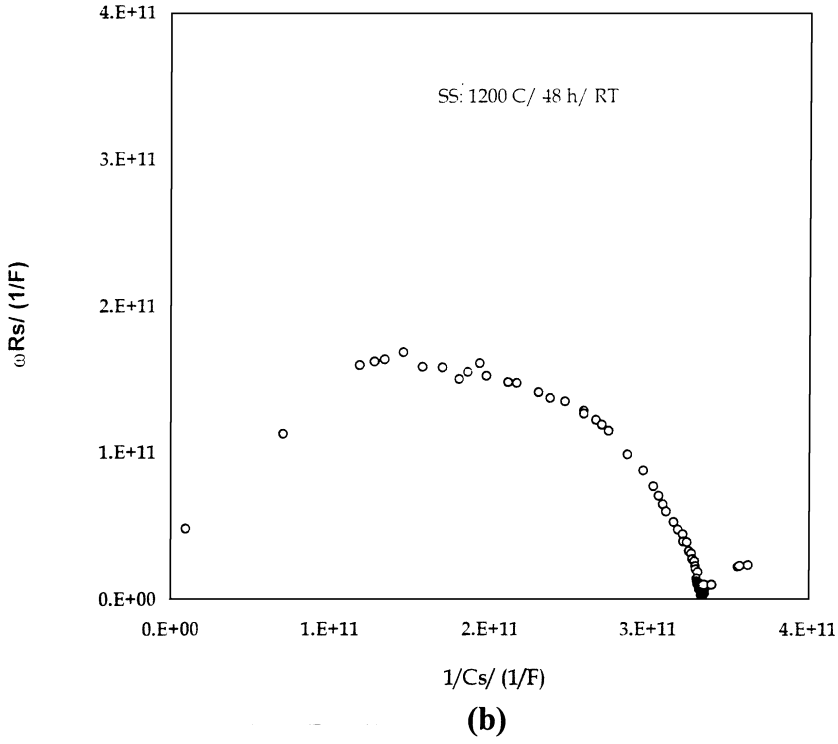
The microstructural features of the starting 'green' $CaSnO_3$ powder as well as the sintered discs were determined by using a JEOL-6400SM scanning electron microscope (Japan). Elemental identification and quantification in different regions of the sintered samples were carried out by using the EDX analyzer (Link eXL, UK) attached to the above SEM machine. Owing to the strong susceptibility of compounds in the Ca-Sn-O systems towards moisture, the calcined powder as well as the sintered discs were always stored in a humidity-free bottle containing anhydrous $CaCl_2$, unless required for microscopic or electrical measurements. It was the sintered discs of $CaSnO_3$ that were employed as DUTs (device under test) for electrical measurements.

2.1.2. Electrical measurements

The electrical data on the sintered samples were acquired over a wide range of frequencies (5 Hz $< f <$ 13 MHz) by using an HP 4192A LF Impedance Analyzer (Yokogawa, Japan) using a proprietary software. Fully automated experimental control was achieved via a desktop PC as the instrument controller. The



(a)

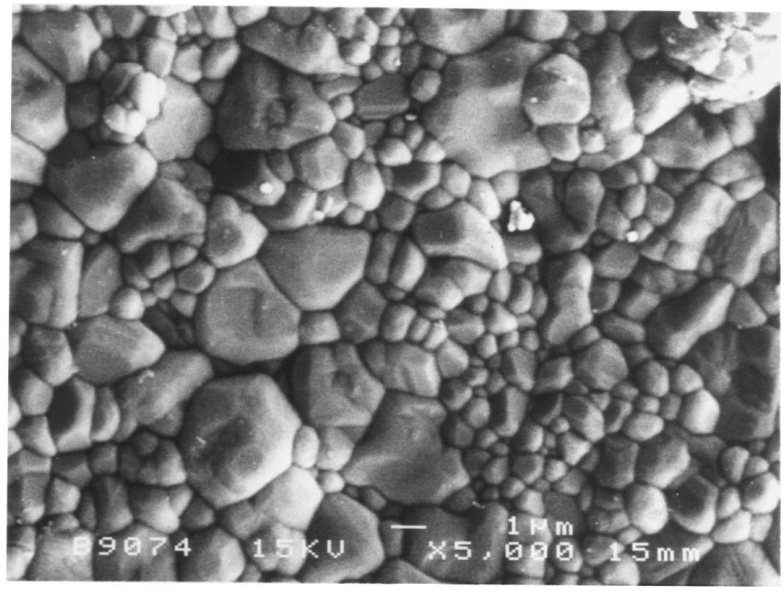


(b)

Figure 2 Room-temperature complex plane plots for $CaSnO_3$ samples sintered at 1200 °C for 48 h. (a) Impedance (Z^*) plot; (b) modulus (M^*) plot of the same data.

small-signal amplitude was about 1 V and the acquired ac data were reproducible with the varying signal voltage. These data were analyzed using a proprietary software package [18]. This package allowed automated data acquisition in any of the desired forms such as, impedance or admittance or phasor, including analyses in the four complex plane formalisms and Bode plane analysis [13, 15, 16]. Necessary electrical parameters were extracted from these representations which employed non-linear least-squared curves-fitting procedure [13–16, 20]. This extraction procedure does not assume or simulate any equivalent circuit configuration *a priori*, which is often done using a commercial software.

Small slices of sintered samples were coated with silver paint (Electrolube Ltd., UK), cured at 500 °C for 2 h, and secured between two highly polished circular stainless steel discs (mounted on Perspex walls) serving as electrodes. The sliced sample was fitted with adjustable screws on both sides of the holder. This



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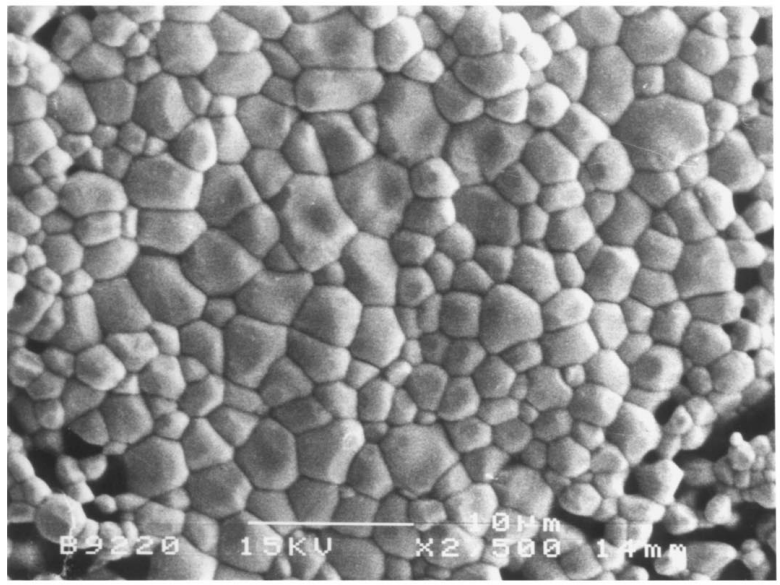


(b)

Figure 3 Microstructural features of the $CaSnO_3$ samples sintered at 1200 °C for (a) 24 h, and (b) 48 h.

arrangement allowed better sample-holding capability in the HP (Hewlett-Packard) accessories. The stainless steel electrodes did not exhibit any contribution to the terminal immittance, as it formed an ohmic contact (resistance $\leq 2\ \Omega$). For the acquisition of ac data at elevated temperatures (above room temperature through 300 °C), an indigenously-designed and fabricated "all stainless steel" sample holder was mounted on an alumina brick ($25 \times 25 \times 10\ mm^3$). To ensure good adherence, high-temperature alumina cement was used and cured at 225 °C for 30 min. Each sample was introduced into the uniform temperature zone of a custom-designed small, low-thermal mass, precalibrated horizontal furnace with temperature fluctuations not more than 1 °C. The furnace was heated to the desired temperature, at a constant rate of 10 °C/min. Adequate amount of time was allowed to equilibrate at the measurement temperature within the sample before the acquisition of ac electrical data. The sample thickness in all the measurements was kept identical.

3. Results and discussion

The analysis of the ac electrical data in four complex planes in the temperature range 25 to 300 °C, revealed semicircular relaxation(s) in the impedance (Z^*), capacitance (C^*), and modulus (M^*) planes for all the samples derived from SSR route and sintered in various t-T (time-temperature) profiles. There was no meaningful feature of the as-acquired data in the complex admittance (Y^*) plane. The inter-relationships among these complex plane formalisms are provided elsewhere [13, 15, 16]. The general features of the ac data included: (a) a single-like semicircular relaxation in the Z^* plane, (b) a semicircle at the high-frequency region including a vertical line parallel to the imaginary

y-axis at the low-frequency region in the C^* plane, and (c) mostly a single-like but in some cases overlapped (like-two) semicircle in the M^* plane.

Fig. 1a–e represents room temperature (25 °C) plots for SSR derived $CaSnO_3$ samples, sintered at 1200 °C for 24 h soak-time. Fig. 1a and b are respectively the total behavior and the high frequency regime relaxation in the Z^* plane. The same data displayed the C^* plane are depicted in Fig. 1c and d. The two distinct relaxations in the M^* plane are depicted in Fig. 1e. Fig. 1a reveals the lumped total resistance $R_{\text{total}}(= R_{\text{g}} + R_{\text{gb}})$ in terms of the length of the chord on the real x-axis. This was found to be in very good agreement with the dc resistance, R_{dc}, measured on the same sample. For instance, Fig. 1a yielded a value of 15.4 MΩ for $R_{\text{total}}(= R_{\text{g}} + R_{\text{gb}})$, which compares well with the dc resistance (R_{dc}) of 15 MΩ. The lumped capacitance, C_{total}, was found to be about 10 pF, which was extracted from the peak-frequency ($\omega R_{\text{s}} C_{\text{s}} = 1; \omega = 2\pi f = 1/\tau$, where τ is time constant or relaxation time) of the semicircular relaxation. Similar exercise with the data in high frequency regime (Fig. 1b), gave 1.34 MΩ as

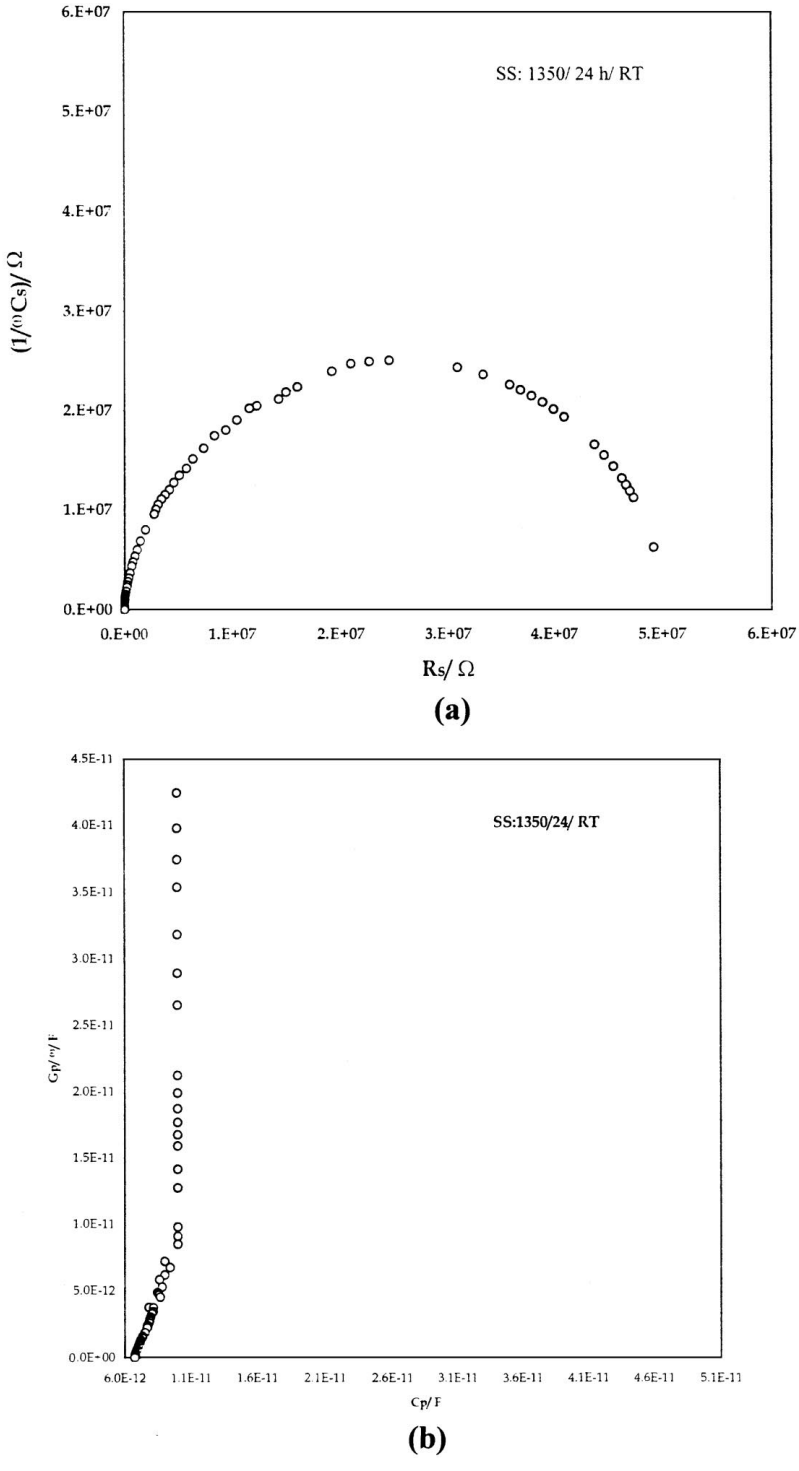
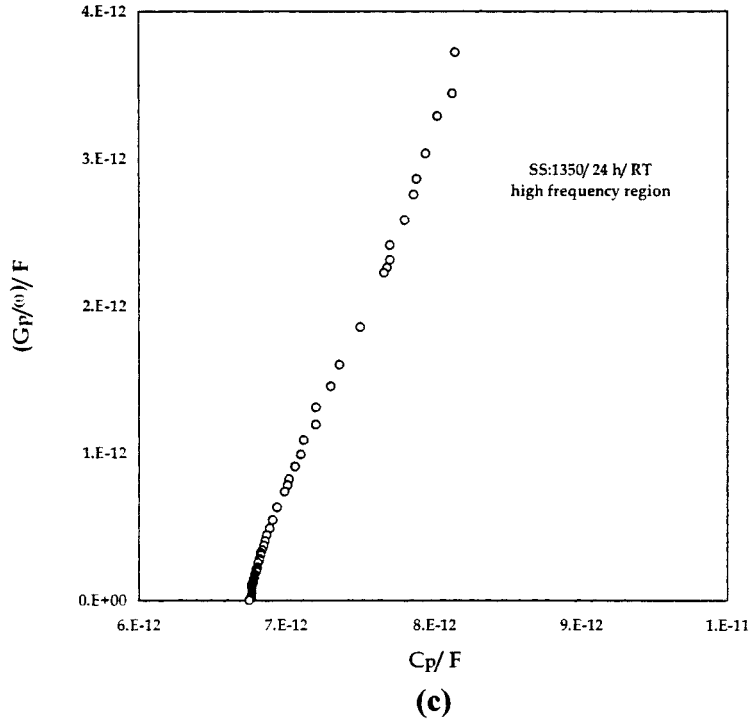


Figure 4 Room-temperature complex plane plots for $CaSnO_3$ sintered at 1350 °C for 24 h. (a) Impedance (Z^*) plot; (b) complex capacitance (C^*) plot of the same data as in (a); (c) exploded view of the C^*-plane plot at high frequencies; (d) modulus (M^*) plot representation of the same data as in (a). (*Continued*).



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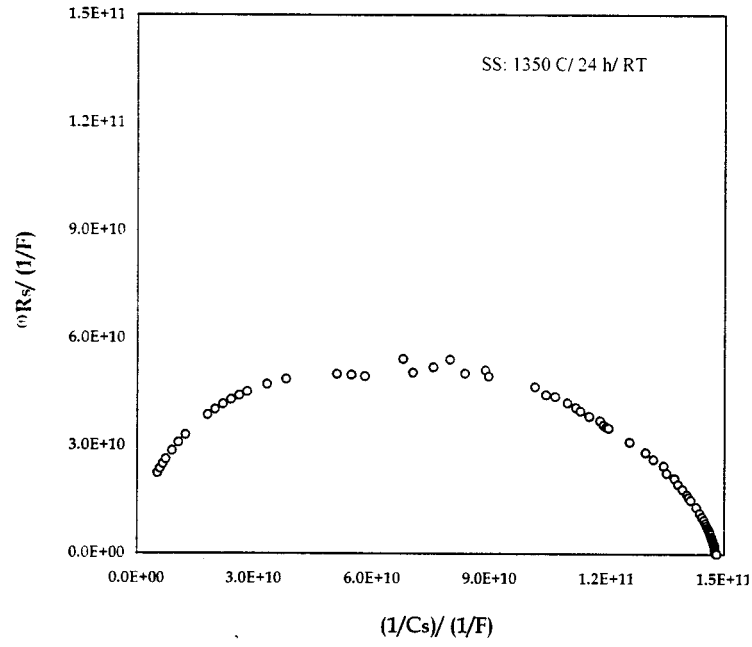


(d)

Figure 4 (*Continued*).

the grain resistance (R_g) and 2.6 pF as C_g. Thus, R_{gb} ($= R_{total} - R_g$) could be computed to be approximately 14 MΩ. The value of C_g corresponds to the dielectric constant [$\varepsilon_r = (C/\varepsilon_0) \cdot (d/A)$, where C is the terminal capacitance, $\varepsilon_0 = 8.854 \times 10^{-12}$ F m^{-1}, d = thickness of the material (m) and A = electrode cross-sectional area (m^2)] of the single crystal of $CaSnO_3$ which is about 6.

When the same ac data are displayed in the C^* plane (Fig. 1c and d), the terminal capacitance neatly resolved into three distinct components:

(a) segment of the straight line parallel to the imaginary (G_p/ω) axis at low frequencies,

(b) high frequency semicircular arc, having a right-intercept on the real (C_p) axis at a point approximately lying on the extrapolation of the straight line, and

(c) a finite left-intercept on the real axis at high-frequencies.

The finite left-intercept (C_2) on the real capacitance axis was found to be about 2.2 pF. This is very close to what has been extracted from the Z^*-plane as C_g which is the dielectric behavior of the $CaSnO_3$ described earlier. Further evaluation of the semicircular relaxation between the high frequency capacitance and the straight line segment yielded the total capacitance ($C_1 + C_2$) which is about 11.5 pF. This is close to what

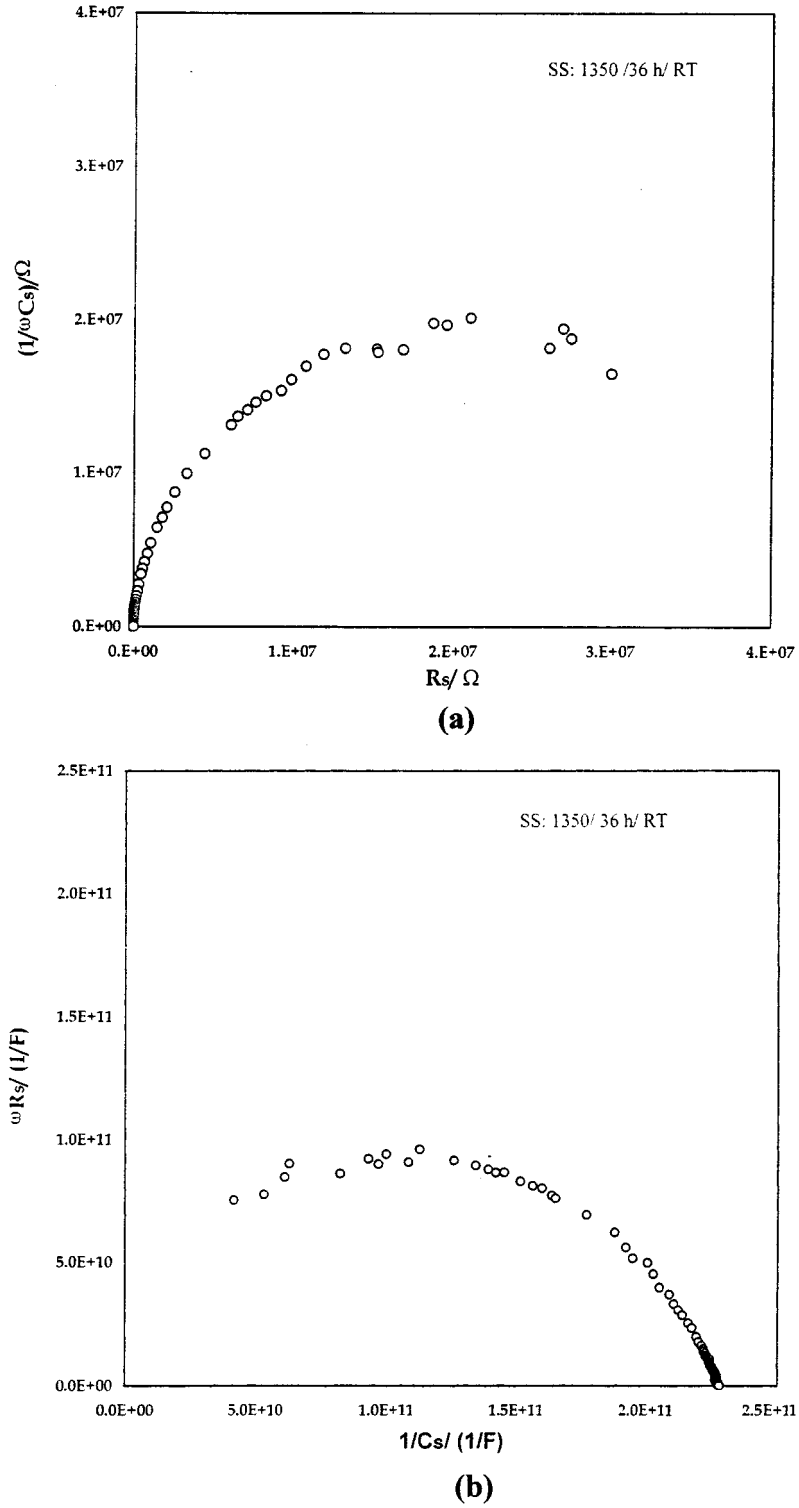


Figure 5 Room-temperature complex plane plots for $CaSnO_3$ sintered at 1350 °C for 36 h. (a) Impedance (Z^*) plot; (b) modulus (M^*) plot.

is obtained in Z^*-plane. The minute difference for C_2 ($= C_g$) and C_{total}($= C_1 + C_2$) obtained from the Z^* and C^* planes is attributed to the non-linear least-squared curve-fitting technique and is found to be reasonable within experimental errors. The parameter C_1 is the trapping capacitance which is a series event (trapping and de-trapping) with the corresponding resistance R_1 and is found to be identical with those of the ZnO-based varistor materials [14]. The trapping capacitance, however, is not treated the same way as is done in ZnO-based varistors [14, 20] because of its less sensitivity as a function of ambient temperature. Thus, the TCC is much smaller for $CaSnO_3$ than for these varistor materials. The terminal admittance at ultra-low frequencies (i.e., near dc limit) appears to be dominated by the dc conductance in the C^*-plane. Such a cut-off response was previously demonstrated for ZnO-based varistors [14]. It is therefore, reasonable to assume that the imaginary part of C^* approached infinity asymptotically at a finite out-of-phase component ($C_{total} = C_1 + C_2$) value, which can be considered as a near static (dc) capacitance as $f \longrightarrow 0$. The corresponding resistance, R_2, associated with the semicircular relaxation, which in fact is the grain-resistance, is found to be 1.5 MΩ. This

value is very close to the value of R_g(1.3 MΩ) obtained from the Z*-plane (Fig. 1b). Combining the value of R_g obtained through C^*-analysis with the foregoing $R_{total}(= R_{dc})$, the lumped grain-boundary resistance is computed to be about 14 MΩ, which matches very well with that obtained from the Z^* plane analysis.

The finite left intercept on the real axis represents a lumped capacitance response of the barrier layer effect originated at the grain-boundary regions and single crystal-like behavior of the grain. However, a comparison of the relative magnitudes of the lumped grain and grain-boundary capacitance, indicates that the contribution of the lumped grains constituting C_2 is likely to be small compared to the barrier layer effect at the grain-boundaries. Thus, the geometric capacitance associated with the barrier layer is the dominating component within C_2, and hence, can be referred to as the barrier layer capacitance. C_2 is predominantly dictated by a 'trap-free' electrical thickness across the grain-boundaries, which sustains major portion of the applied electrical field under a non-equilibrium condition. The electrical field drop across the lumped grains is much smaller than the electrical field drop across the lumped grain-boundary electrical thinness. This is due to the large dc conductivity and is attributed to the donors within the lumped grains. The bulk dielectric behavior of the lumped grains mentioned earlier is, thus, incorporated into C_2. This bulk property can be isolated at ultra-high frequencies (in this case exceeding 13 MHz), exhibiting a lead-electrode related post-inductive response as found in ZnO-based varistors [14]. However, this is not done here due to the limitation of the instrument. The C^*-plane relaxation does not give the grain bulk resistance (R_g); it can only give C_g. Likewise, the grain boundary resistance (R_{gb}) in C^*-plane is masked under R_{dc} (or R_{total}) in the Z^*-plane. This shows that grain and grain-boundary resistances are different from each other, otherwise dual relaxation in C^* as well as in Z^* plane would not have been observed. Also, this is exactly the case as the aforementioned analyses of the ac data in the two complex planes have demonstrated. Some relevant conditions for such dual representations have been postulated by Seitz [21]. Thus, the purpose of the multi-plane analytical technique approach advocated in references 13 through 16 is conducive to the understanding of the complex material system.

A further examination of the above data analysis technique is applied to the two overlapping (in the frequency domain) semicircular relaxations in the M^* plane (Fig. 1e). The curve-fitting approach of these two overlapped semicircles yielded values of 8 pF and 13 MΩ for C_{gb} and R_{gb} respectively, in the low frequency domain. 13 MΩ is very close to 14 MΩ which is obtained from the Z^*-plane for R_{gb}. Due to the overlapping response, this value could not be resolved very precisely. Thus, the corresponding capacitance 8 pF is somewhat lower than what was found in the Z^*-plane. However, 3 pF is obtained for the lumped grain-capacitance (C_g) from the high-frequency domain (Fig. 1c). This is in close agreement with the previous analyses of 2.6 pF from Z^* plane and 2.2 pF from C^* plane discussed earlier. The value of R_g, determined from the peak frequency condition ($\omega R_g C_g = 1$) in the M^* plane is slightly lower. The difference between the values of R_g obtained from Z^* and M^* planes could again be attributed to the errors in the curve fitting procedure which is within the tolerance limit of the experimental procedures.

The room temperature ac data acquired on $CaSnO_3$ samples, soaked for 48 h at 1200 °C, showed a single lumped behavior in the Z^*-plane while there were two distinct relaxations in the M^*-plane, as shown in Fig. 2a and b respectively. The Z^*-plane yielded a semicircle with left intercept on the real axis near to the origin (∼0) and the chord length (right intercept = R_{total}) equal to 84 MΩ. The corresponding lumped capacitance (C_{total}) was computed to be 3.2 pF. These two values are in agreement with those extracted from two relaxations in the M^*-plane. Thus, increase in soak-time from 24 to 48 h, has caused an increase in the total resistance, R_{total}, to about 85 MΩ from about 15 MΩ (obtained in Fig. 1 discussed earlier). This indicates that the total resistance was grain boundary dominated. Such an enhancement in the resistance is possibly related to the improved densification via better compaction of the grain-to-grain contact. This implies more well-defined grain boundaries via the uniformity in the grain-size distribution when compared to the samples sintered at 1200 °C for 24 h. Fig. 3 demonstrates these microstructural features. The abnormal grain growth and rather broad grain size distribution in samples sintered for 24 h at 1200 °C could also be responsible for slightly higher total capacitance value, compared to that in samples soaked for 48 h, which resulted in more or less monosized grains with uniform grain boundary thickness. This speculation is strengthened by the fact that while the total resistance in samples sintered for 60 h at 1200 °C increased to 261 MΩ, the corresponding capacitance was 4.4 pF, nearly same as that in the samples with 48 h soaking at the same temperature. It can therefore, be concluded that the degree of homogeneity or heterogeneity of the trap levels at the grain boundaries was not affected in samples soaked for 48 h or more at this temperature. In all these cases, the lumped semicircular relaxations in the Z^* plane are depressed, i.e., the center of the semicircle lies below the x-axis, exhibiting a finite depression angle (θ). This depression is indicative of the distribution of the relaxation processes and a non-Debye behavior of the material. This is also an indication of the degree of heterogeneity in the operating electrical paths which is responsible for the departure from Debye characteristics. This, nevertheless, is an expected trend in polycrystalline devices [13–16, 20]. However, the invariance of θ (11.5° , 10.6° and 10.8° for samples sintered at 1200 °C for 24, 48 and 60 h respectively) with soak-time, suggests that the degree of heterogeneity in the lumped electrical paths is nearly invariant with soak-time at a given sintering temperature. This finite but small depression angle indicates that the departure of the ideal Debye response of the overall electrical paths, operative between the opposite electrodes, is not large.

The room temperature electrical data for the samples sintered at 1350 °C for 24 h also showed similar

relaxations in Z^*, C^* and M^* planes and are depicted in Fig. 4a–d. The curve-fitting of the near ideal lumped relaxation in the Z^* plane (Fig. 4a) yielded $R_{\text{total}}(= R_g + R_{gb})$ of about 50.8 MΩ and C_{total} of about 10.2 pF. In this case, the depression angle in the Z^* plane is about 2.6°. The lumped grain and grain-boundary resistances match very well with the R_{dc} value of 49.2 MΩ which is also in good agreement with the value of 47.1 MΩ, obtained by curve fitting of the same data in M^* plane (Fig. 4d). The dispersion of the ac data in the C^* plane was akin to that observed in the case of samples sintered at 1200 °C, though the semicircle in the higher frequency regime less pronounced. The finite left intercept (C_2) on the real capacitance axis was found to be about 6.8 pF, whereas the curve fitting of the semicircular relaxation between the high frequency terminal and the straight line segment yielded the total capacitance ($C_1 + C_2$) to be about 9.4 pF which agrees well with the C_{total} of 10.2 pF obtained by Z^* plane fitting.

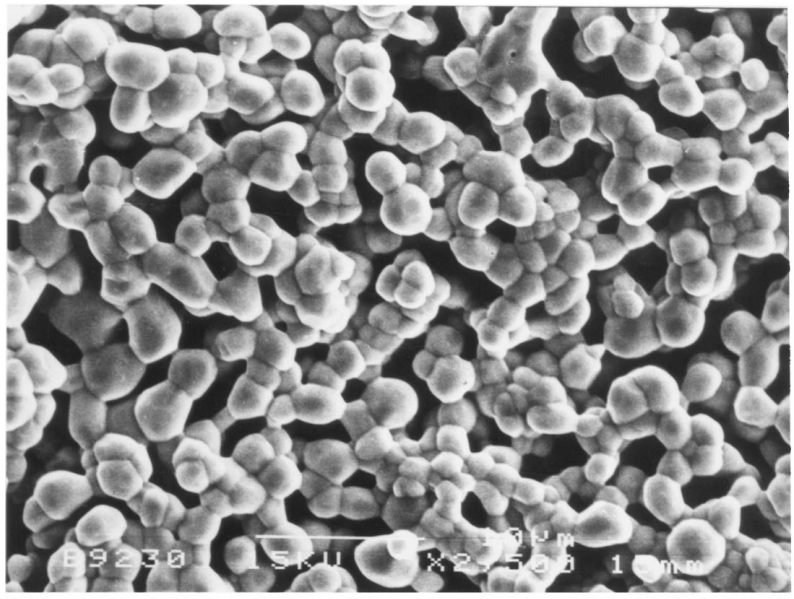
The C^* plane analysis also yielded a value of R_2 ($= R_g$) equal to 14.6 MΩ. Combining the data extracted from the Z^* and C^* planes, the grain-boundary resistance ($= R_{\text{total}} - R_{\text{grain}}$) is found to be about 35 MΩ. Two interesting features of this analysis are worth highlighting here. First, the total sample resistance increased from 15 MΩ (in 1200 °C sintered samples) to 50 MΩ; the grain boundary resistance was also the dominating fraction of the total, being almost twice that of the grain resistance, compared to being about 14 times in the samples sintered at 1200 °C for the same duration. Second, the total capacitance remained almost invariant to the temperature of sintering (∼10 pF). This suggests that the total barrier layer thickness which is inclusive of the electrical field falling region within the sample is nearly invariant with the sintering temperature. In fact, the ac small-signal electrical field (1 V) is distributed over this thickness within the sample. Furthermore, this invariant trend implies that the nature of conduction mechanism, charge carriers, trapping parameters, etc. are not altered in these samples.

The room temperature ac data on samples sintered at 1350 °C for 36 h yielded single-like lumped relaxation in both Z^* and M^* planes as shown in Fig. 5a and b. The extracted circuit elements from the Z^*-plane ($R_{\text{total}} = 50.1$ MΩ; $C_{\text{total}} = 6.6$ pF) match very well with those from the M^* plane ($R_{gb} = 37.2$ MΩ and $C_{gb} = 9.9$ pF; $R_g = 7.5$ MΩ and $C_g = 8$ pF) as well as with R_{dc} value of 49.8 MΩ. It is evident that the total resistance of the sample remained nearly constant as soak time was increased from 24 to 36 h at 1350 °C. The lumped contribution of the grain boundaries increased marginally with a slight decrease in grain resistance. The microstructural features of samples sintered at 1350 °C for 24 and 36 h are shown in Fig. 6a and b, respectively. There is a definite grain growth in samples sintered for longer duration, attended by a downsizing of the grain-size distribution. However, the density of the sintered bodies in the two samples (72 and 78% respectively, as measured by Archimedes method) is nearly identical, considering the amount of respective porosity that still exists in both the samples. The ac data on samples sintered at 1350 °C for 48 h did not show sharply different characteristics than those exhibited by the samples with soak-time 24 and 36 h as discussed above, using multi-plane criteria [13–16]. These results are shown in Fig. 7a–d. However, there is a drastic decrease in the total resistance, extracted as lumped quantity from Z^* and M^*-planes, where the relaxation was observed in the form of a single-like semicircle in the entire measurement frequency range.

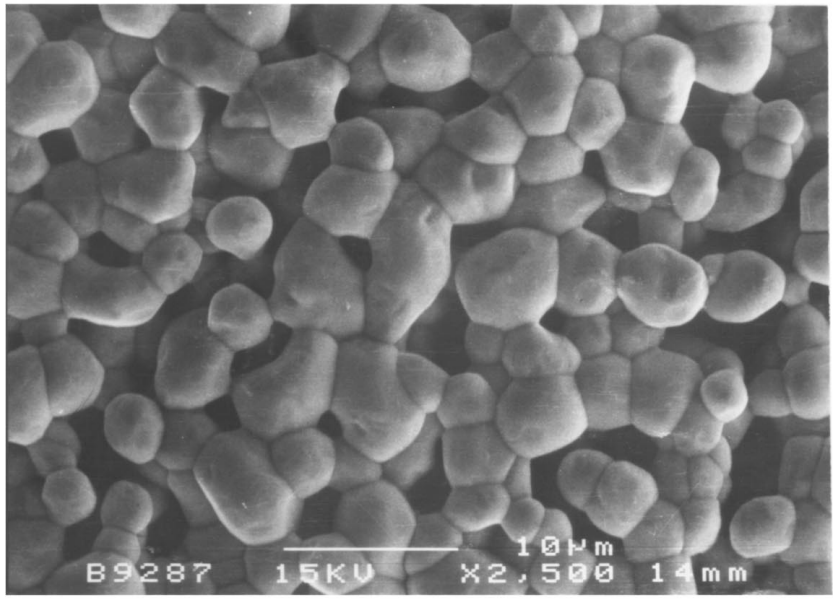
The extracted parameters in this case were as follows: $R_{\text{total}} = 16.7$ MΩ; $C_{\text{total}} = 7$ pF and $\theta_{\text{total}} = 10.6°$ from the Z^*-plane, agreeing very well with $R_{\text{total}} = 16.5$ MΩ; $C_{\text{total}} = 5.8$ pF and $\theta_{\text{total}} = 8.2°$ from the M^*-plane. The dc resistance (R_{dc}) of the sample was 17 MΩ. When the LP/CPA technique was applied to the same data in the C^*-plane, the finite left intercept (C_2) on the real x-axis was found to be 5.7 pF, while the semicircular relaxation between the high frequency terminal and the low frequency asymptotic segment yielded the total capacitance to be 6.2 pF, which agrees very well with the C_{total} from Z^*- and M^*-planes (7 and 5.8 pF, respectively). The analysis also yielded 10.2 MΩ for $R_2(= R_g)$; this gives the value of 6.5 MΩ for grain boundary resistance, $R_{gb}(= R_{\text{total}} - R_g)$.

The analytical criteria indicate that the capacitance characteristics of the $CaSnO_3$ samples sintered at 1350 °C for the duration ranging between 24 to 48 h did remain nearly invariant. The sample became more conductive at the longer soak-time. This could be ascribed to significant (nearly theoretical) densification and elimination of the pores as shown in Fig. 6c. In addition, nearly constant and similar values of the depression angles (10° or so), further strengthened the view that the conducting paths and mechanisms remained uninfluenced by the sintering schedules in this solid-state derived material.

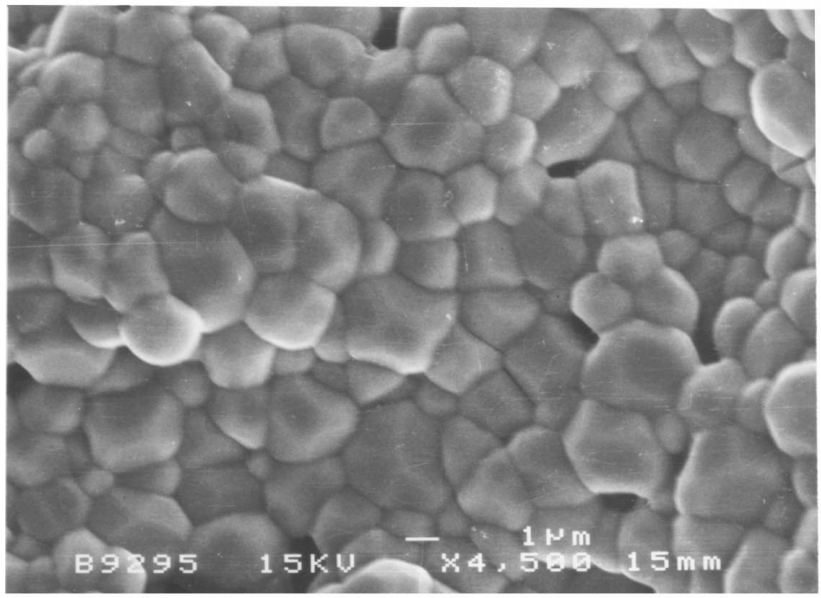
Since the complex plane formalisms (as demonstrated above) allow the extraction of more information, the Bode plots are not presented here. The information obtained from the Bode plots are verified, and found to be contained in these formalisms in terms of vivid circuit elements including their Debye/non-Debye responses within the electrical paths. However, the features of the Bode plots between room temperature and 300 °C, over the range of measurement frequency, can be summarized as: (i) the sample capacitance remains invariant with frequency over a wide range both at room and elevated temperatures up to 300 °C, (ii) in the same range of frequency, the capacitance is invariant but increased as the soak-time increased, and (iii) the average magnitude of capacitance at these two temperatures is nearly unaffected (a few pF) for the samples sintered at 1200 °C and/or at 1350 °C for duration spanning between 24 to 48 h. This is in contrast to the observations reported by Parkash *et al.* [10], Mandal *et al.* [11] and, Upadhyay *et al.* [12] wherein a strong frequency dependence of capacitance could also be seen at the three individual frequencies (1, 10 and 100 kHz). The capacitance provided by these investigators is the terminal capacitance resulting from a single stage sintering. Such a demonstration might have either led to inconsistent microstructural development in conjunction with



(a)



(b)



(c)

Figure 6 Microstructural evolution in $CaSnO_3$ samples sintered at 1350 °C for (a) 24 h, (b) 36 h, and (c) 48 h.

the development of the frequency-dependent trapping states due to the specific sintering schedules in their samples or, variable processing method that might be drastically different from that reported here. That fact is that the role of traps (overall in the grain- boundary regions) seems to have a greater influence on their samples than the samples presented in this work. It is worthwhile nothing that the ZnO-based varistor materials are heavily dominated by the trapping states and eventually play a key role in the electrical response despite a large variation in the sintering schedules combined with soak-time [20]. Strong frequency-dependent behavior has also been documented for these varistors via the complicated Mott-Schottky response [14].

Near non-invariant behavior of permittivity (ε') in the temperature range of electrical measurements (25–300 °C) exhibited by samples sintered at 1200 and 1350 °C for various duration, supported the fact that a reliable capacitor with very low temperature coefficient of capacitance (TCC) has been realized. Since

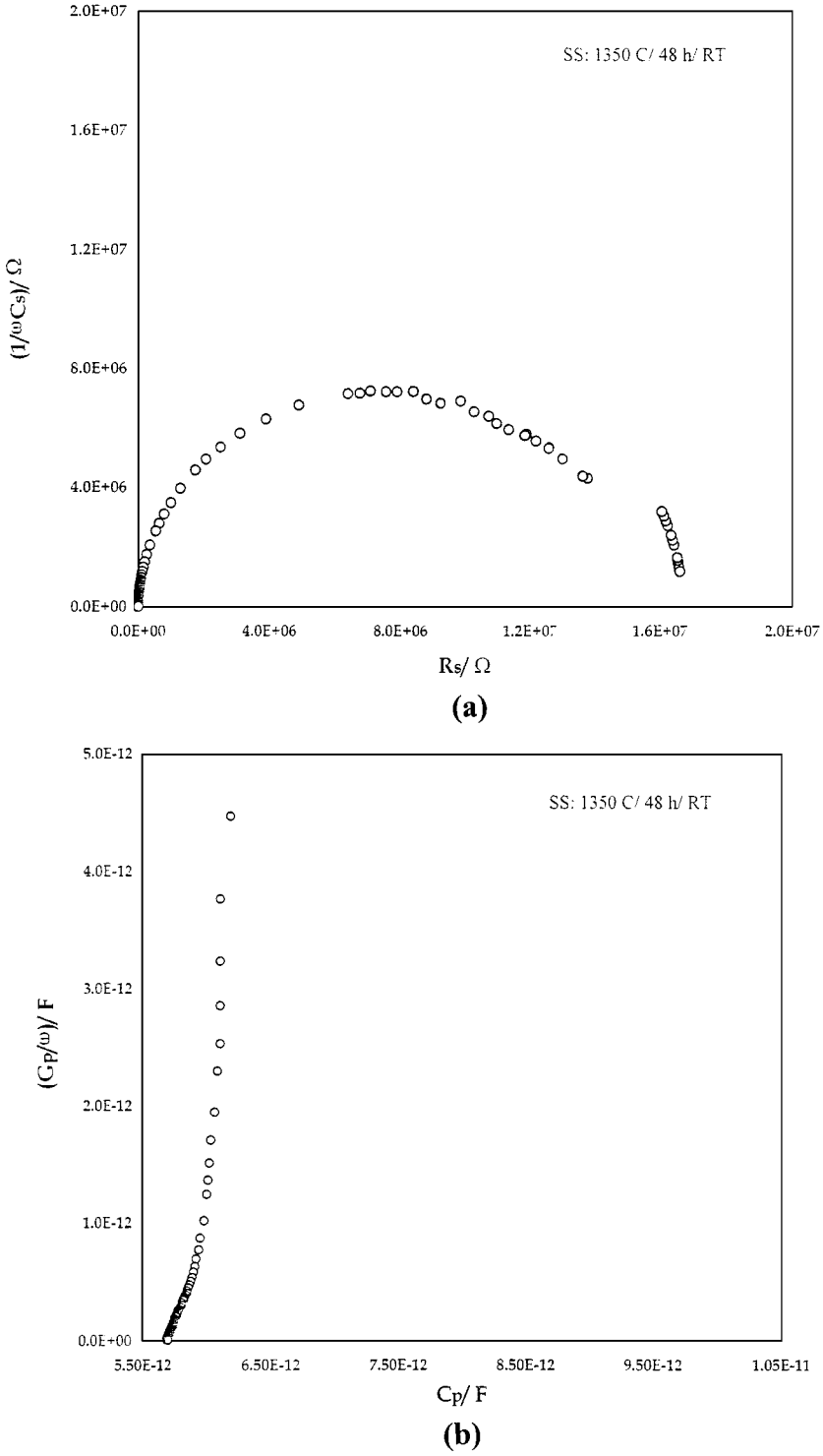


Figure 7 Room-temperature complex plane plots for $CaSnO_3$ sintered at 1350 °C for 48 h. (a) Impedance (Z^*) plot; (b) complex capacitance (C^*) plot of the same data as in (a); (c) exploded view of the C^*-plane at high frequencies; (d) modulus (M^*) plot representation of the same data as in (a). (*Continued*).

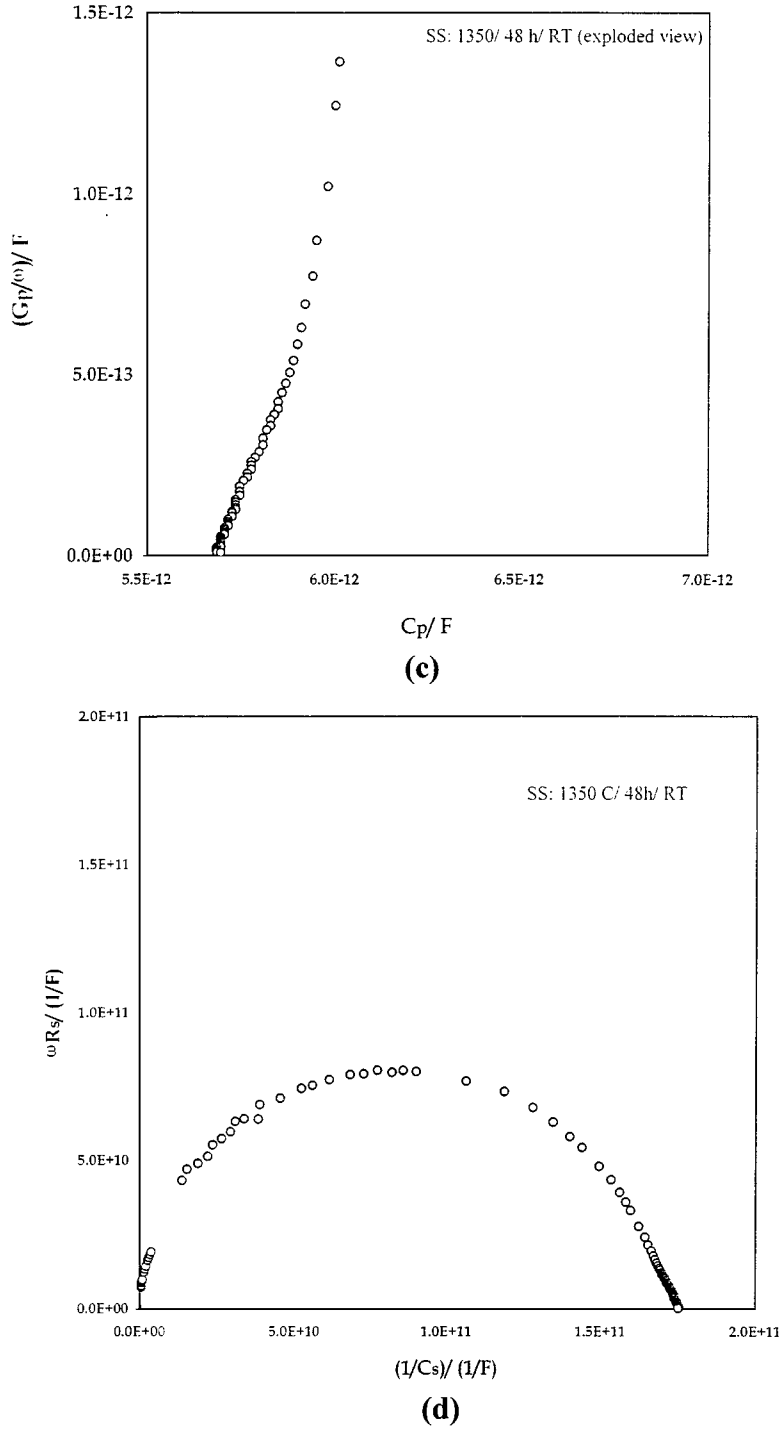


Figure 7 (*Continued*).

capacitance C and permittivity ε' are equivalent except for the geometrical factors (thickness and cross-sectional area of the sample) and the constant ε_0, ε' is essentially a normalized parameter containing the geometrical factors and ε_0. Therefore, the as-measured capacitance C was directly used to generate corresponding Bode plots. Some typical Bode plots (log C vs. log f) are shown in Fig. 8. For each of the samples investigated, a steep transition in capacitance is seen at the low end of the measurement frequency. This response could be ascribed as the possible polarization effects at the electrode at these frequencies. The dielectric loss (tan δ) is also found to be too small over several decades of frequency in the temperature range 25–300 °C. Some typical loss tangent plots as a function of frequency are shown in Fig. 9. Thus, this material is exhibiting potential as a promising candidate for the capacitor element possessing an ultra-small value of TCC. The behavior of these two parameters measured in the range 25 to 300 °C remained almost identical except for some scatter in the measurement presumably due to the polarization effect. It can be seen from Fig. 8, that an average value of 2 to 3 pF and 3 to 7 pF can be assigned to $CaSnO_3$ capacitors sintered at 1200 and 1350 °C respectively, over the range 25 to 300 °C. For further minimization of the scatter in the capacitance value, more detailed sintering within short intervals of soak-time is recommended.

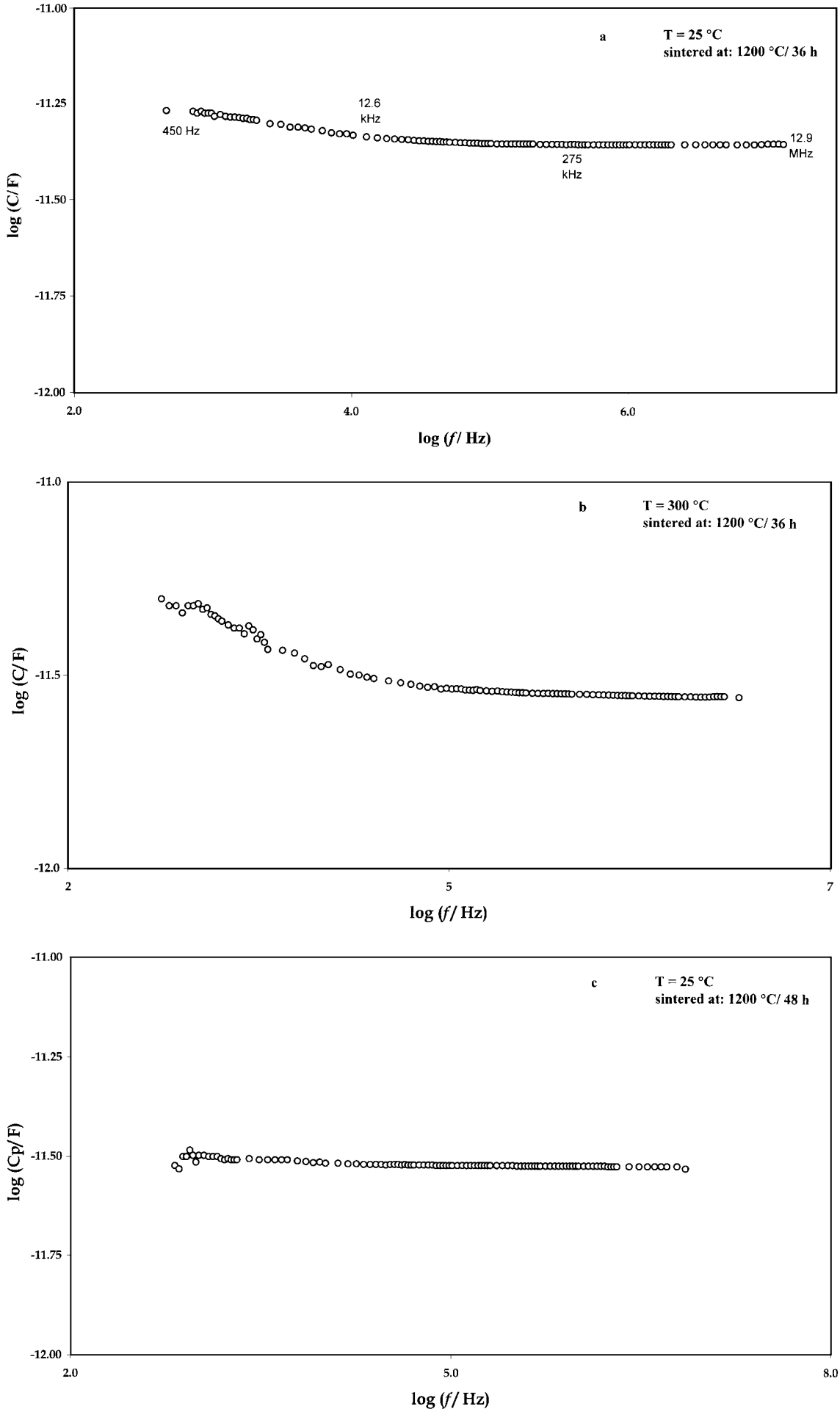
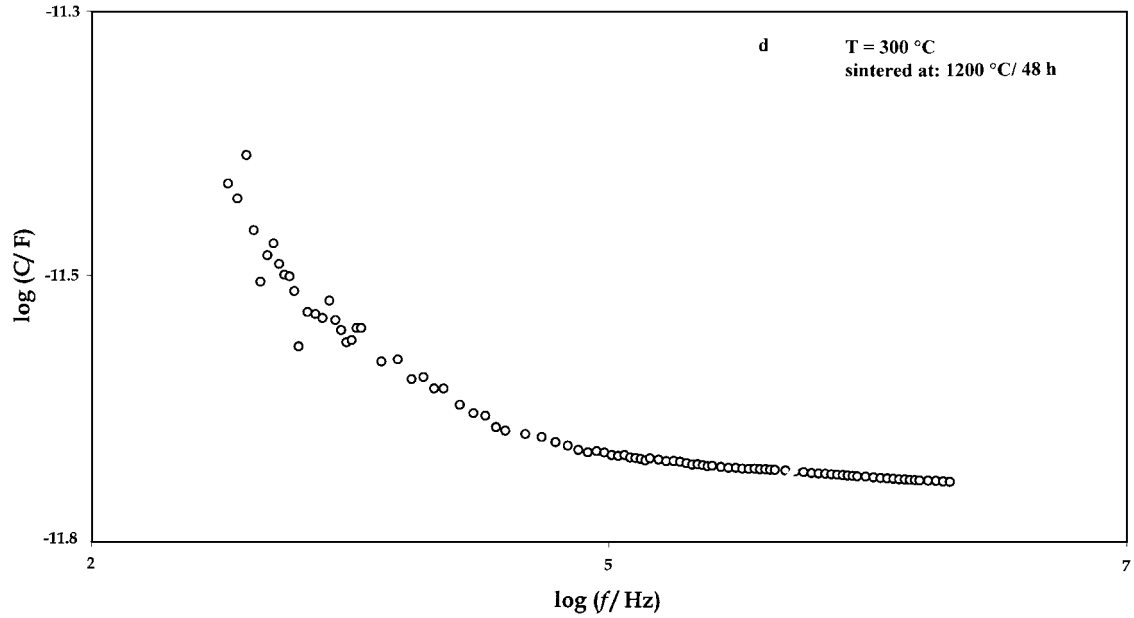
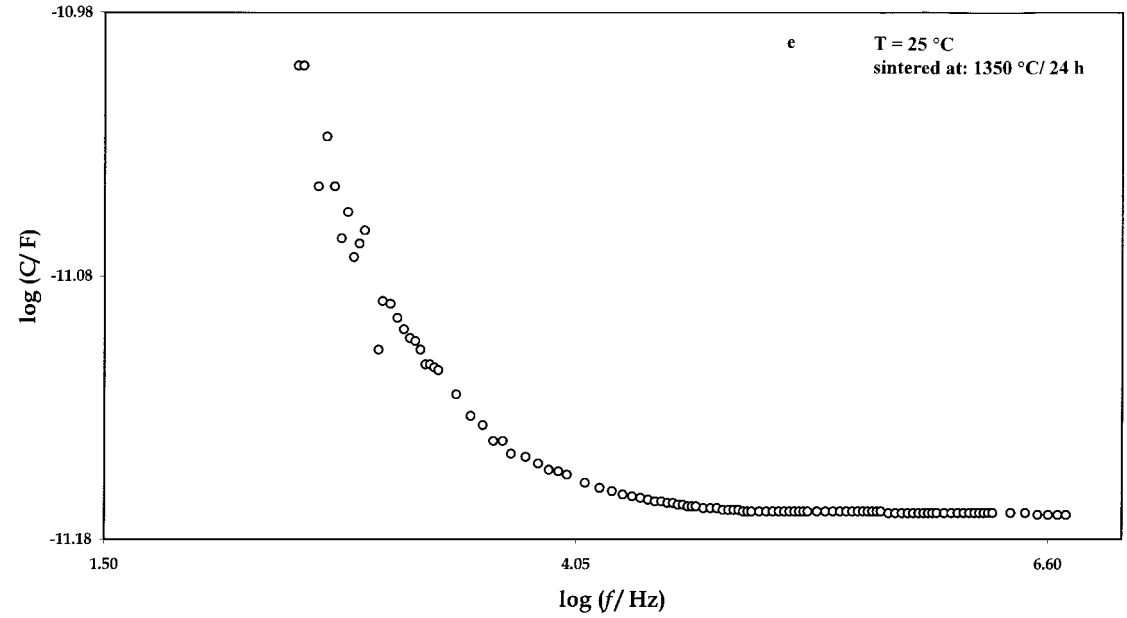
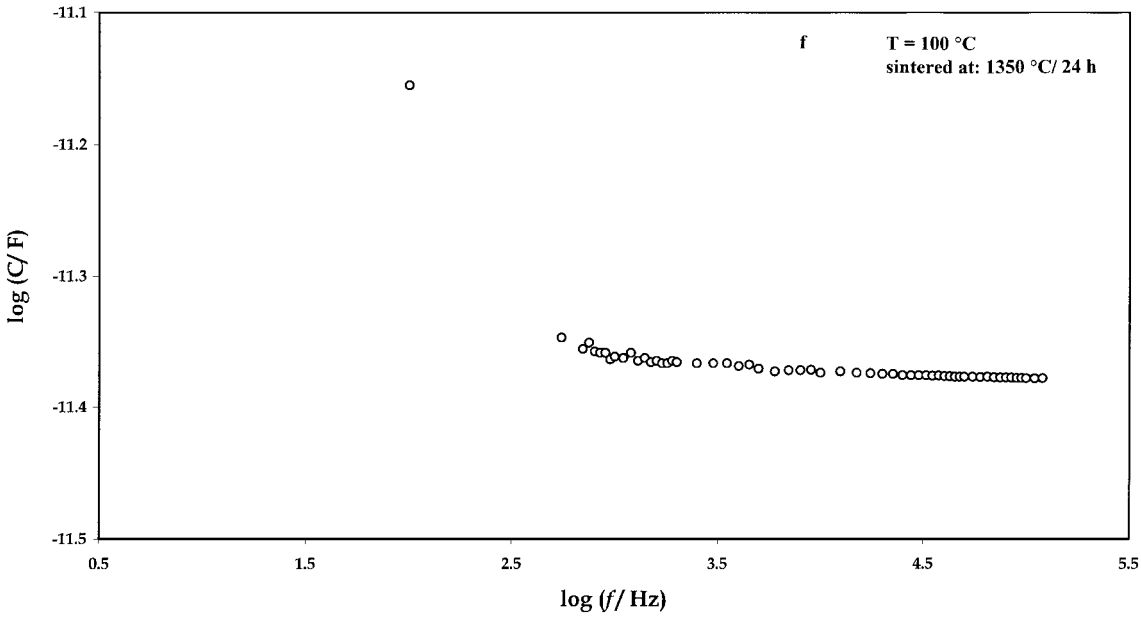


Figure 8 Variation of as-measured capacitance (non-normalized permittivity ε') at different temperatures as a function of frequency in sintered $CaSnO_3$ samples. (*Continued*).







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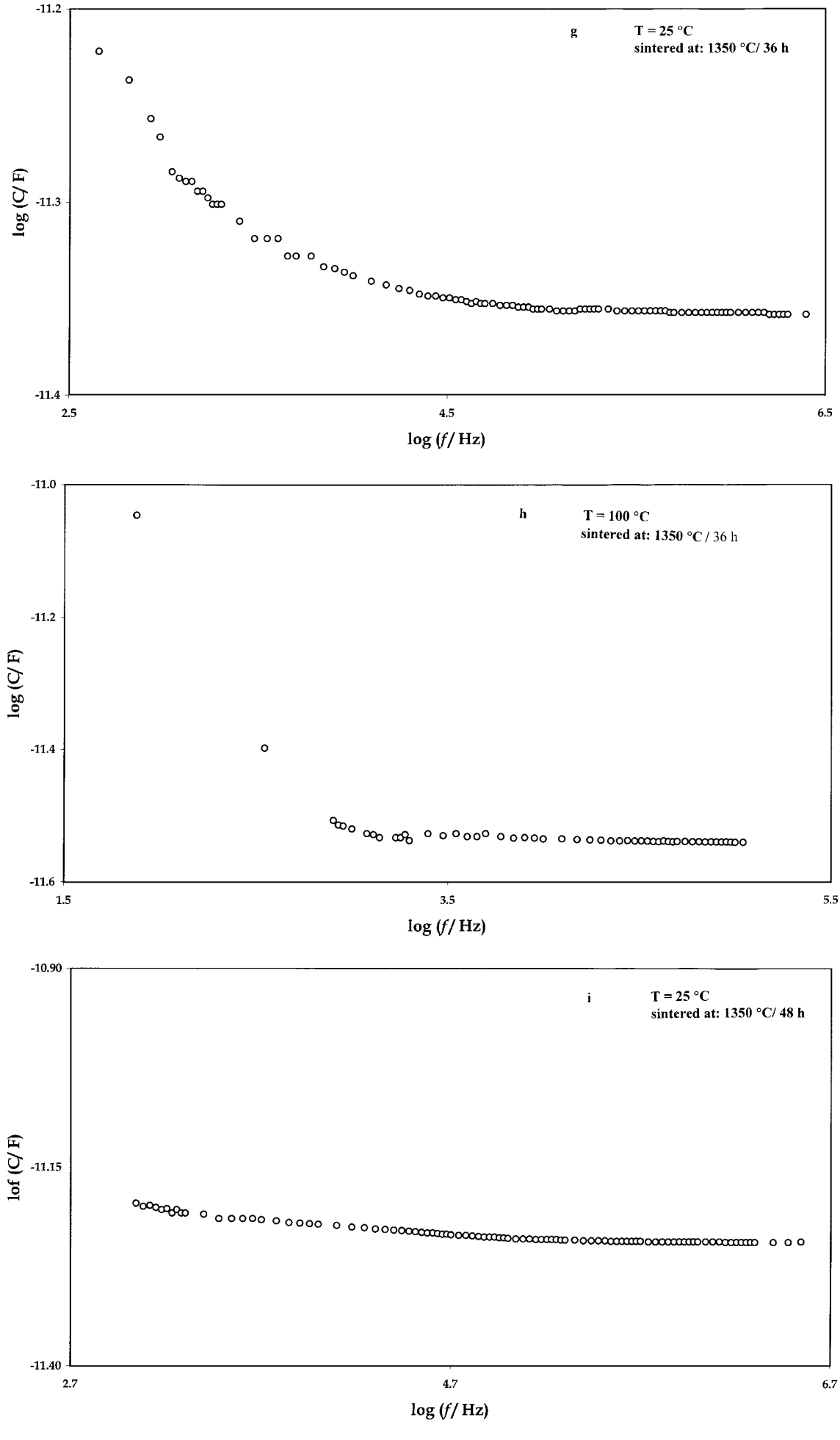

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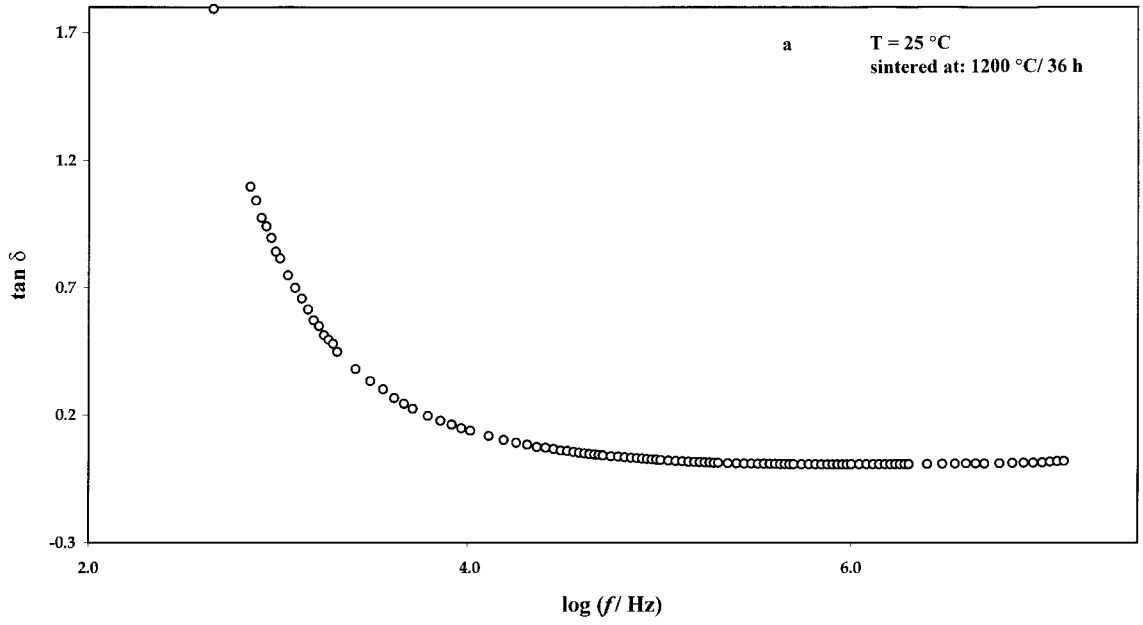
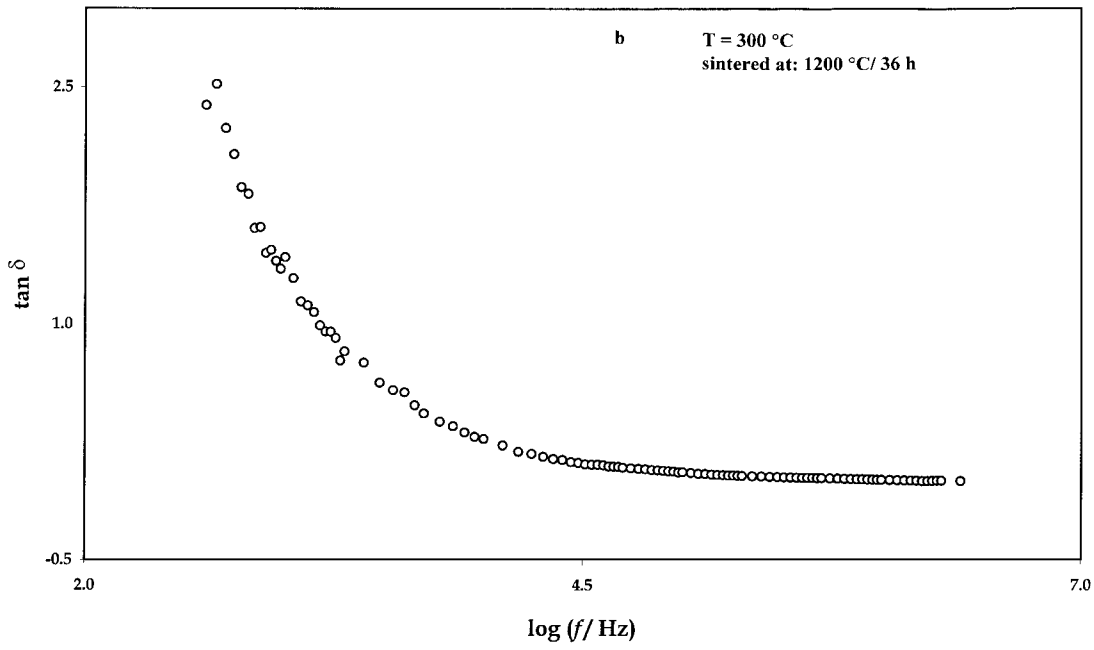




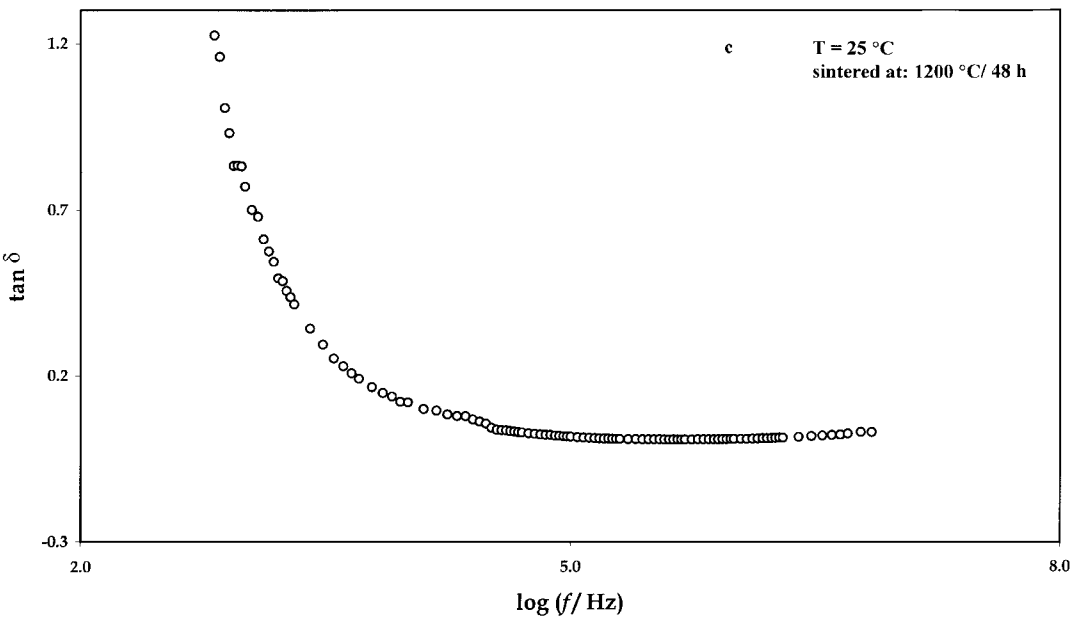
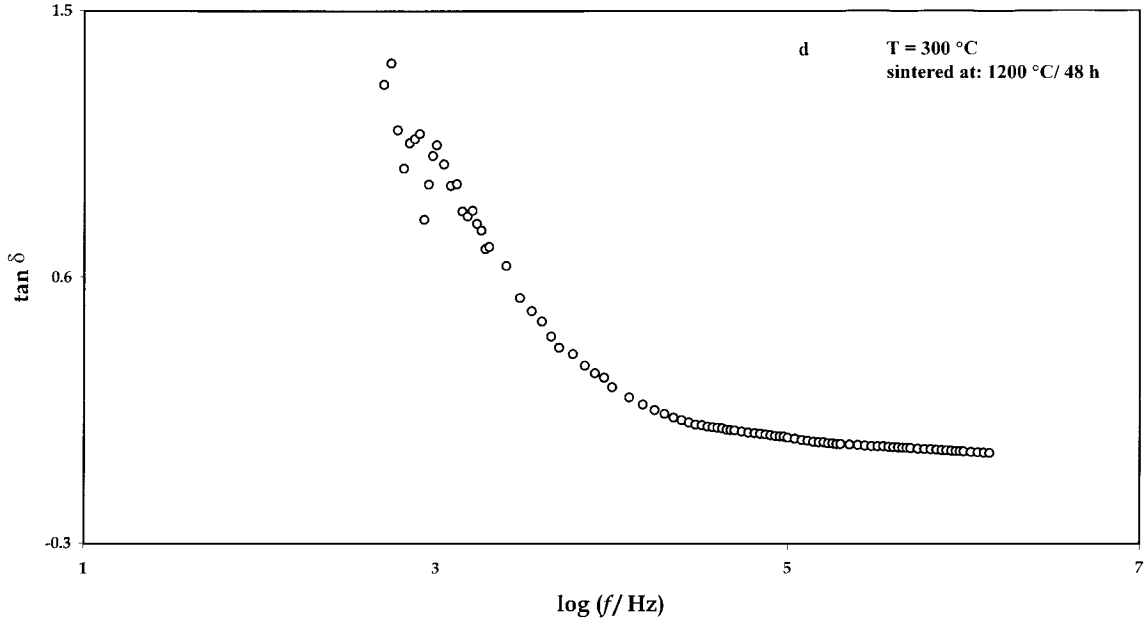
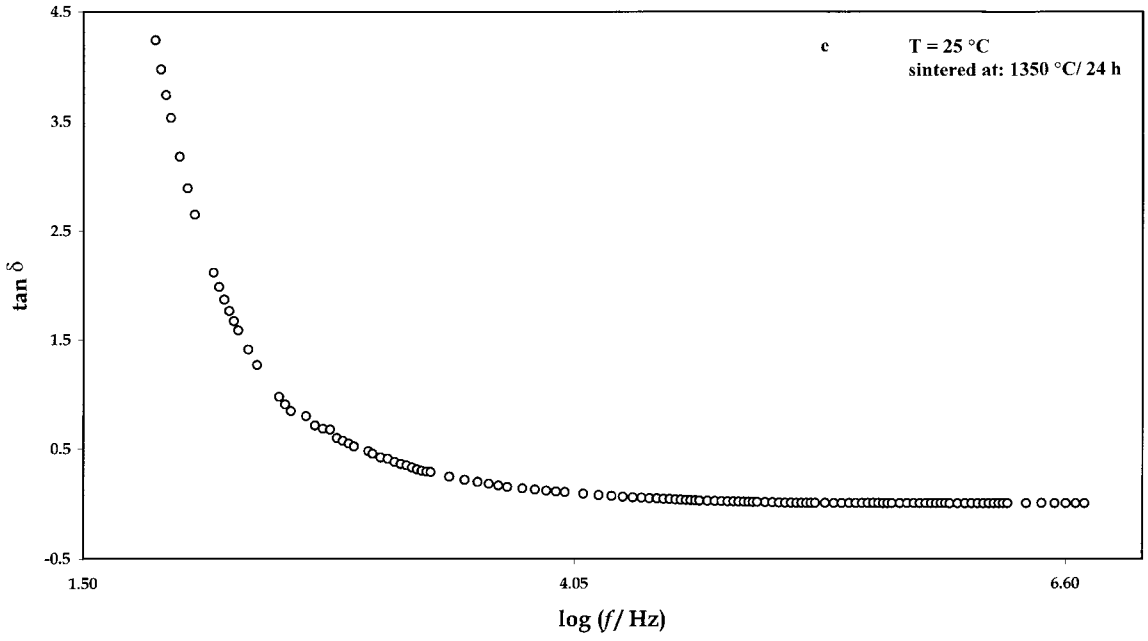
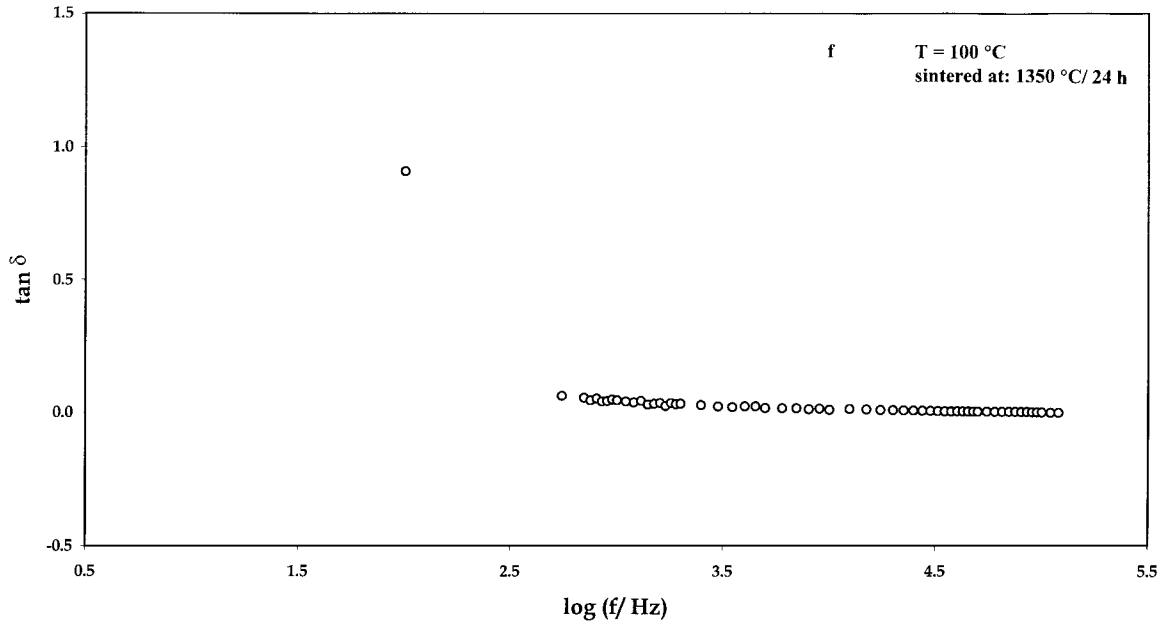


Figure 9 Frequency dependence of loss tangent ($\varepsilon''/\varepsilon'$) at different temperatures in $CaSnO_3$ samples with various sintering history. (*Continued*).







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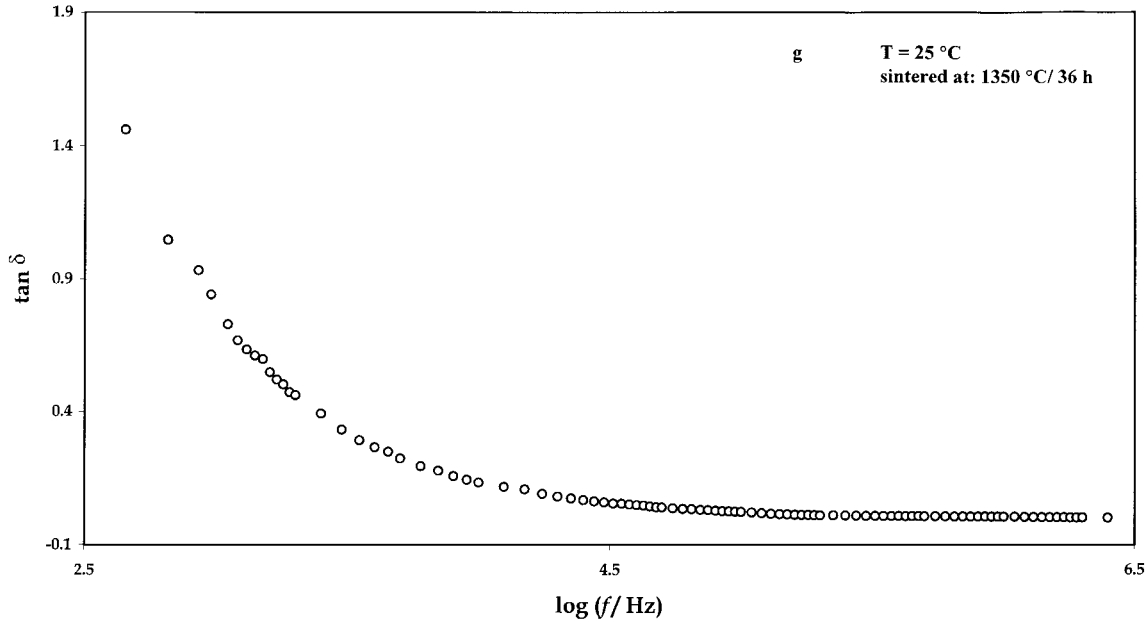

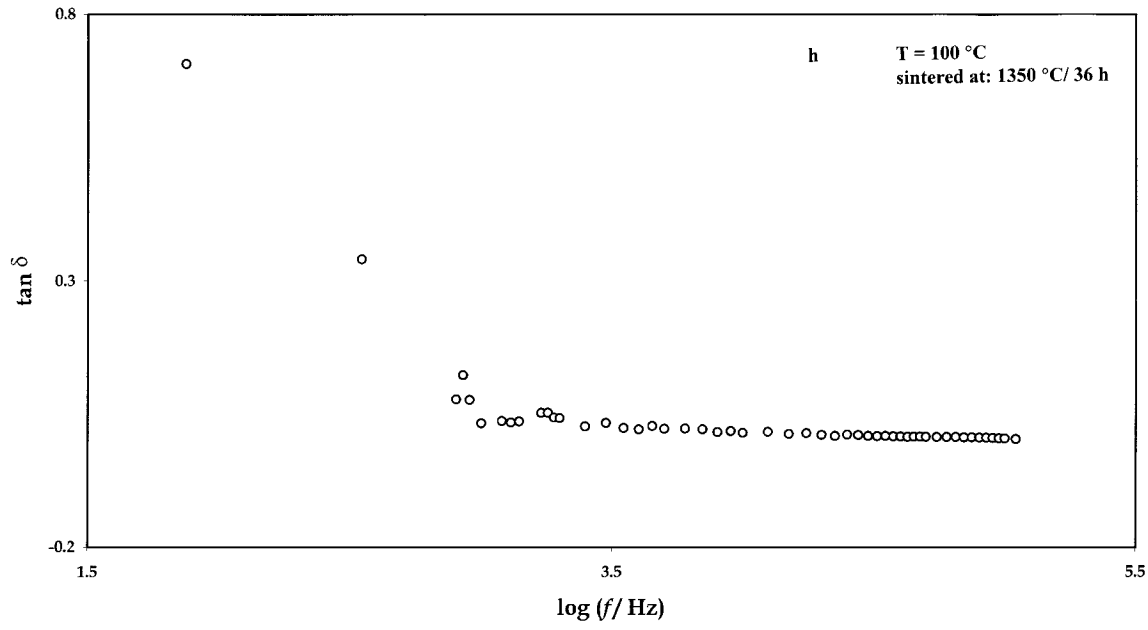

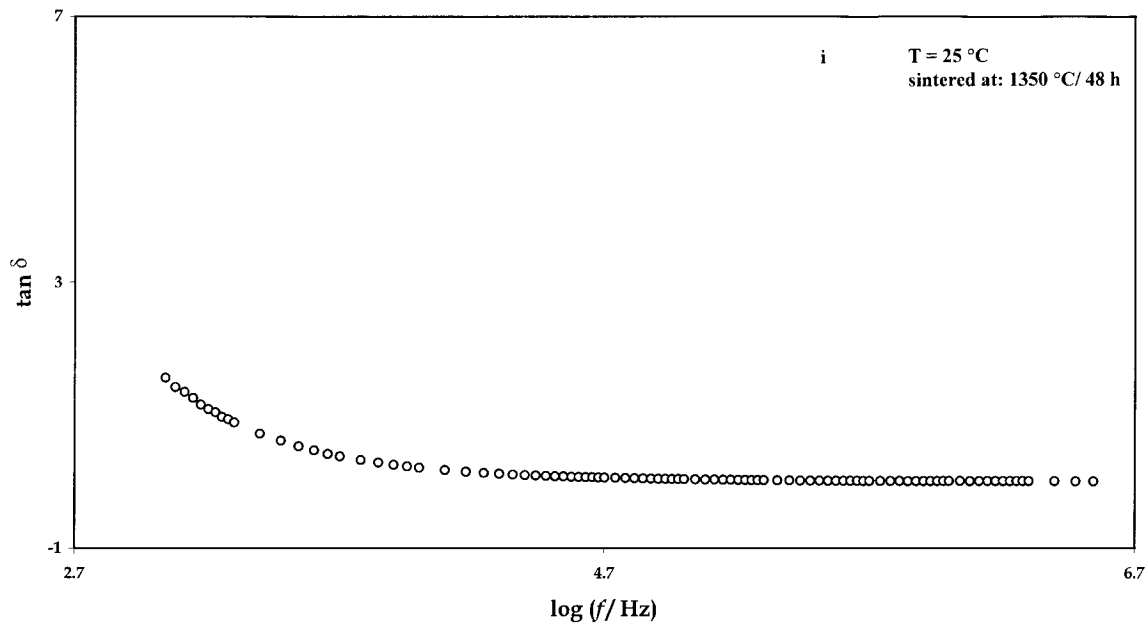

Figure 9 (*Continued*).

4. Equivalent circuit model

In the light of the above analytical approaches, employing multi-plane analytical technique and using the phenomena related to these representations, a methodical list of representations for this material system can be prepared. The Z^*-plane analysis yields lumped grain as well as lumped grain boundary response, where in most cases single-like semicircular relaxation is observed. In many cases such responses could be resolved analytically in conjunction with the relaxation observed in the M^*-plane. The relaxation in the C^* plane represents the trapping contribution within the electric filed falling regions of the samples. Thus, there is a dual perspective in the electrical response and therefore, ideally, there is a duality in the equivalent circuit representation as well. This duality does not lead to controversy but helps in understanding the operative phenomena within the material system. Thus, both circuits are valid under specific conditions and viewing perspectives. The judgment depends on the visibility of the frequency response of the material. Considering dual representation of the equivalent circuit model, the electrical paths operative in this material can be viewed in the following ways.

The Z^* plane relaxation may be expressed either (i) in the form of one equivalent parallel resistor-capacitor (R-C) combinations, where the response was in the lumped form (Fig. 10a) or, (ii) in the form of two equivalent parallel resistor-capacitor (R-C) combination connected in series, where the contribution of grains and grain boundaries could be analytically separated with the help of simultaneous relaxation in the reciprocal plane (M^*); R_1-C_1 combination represents the grain, and the R_2-C_2 combination represents the grain boundary (Fig. 10b).

The semicircular part of the C^* plane relaxation, as is well known, is an indication of the relaxation of the series R-C circuit combination. This is shown in Fig. 10c which is essentially the series in-phase and out-of-phase trapping event, within the electrical field falling regions comprising of the grain boundary electrical thickness. The capacitance and resistance of the $CaSnO_3$ grains are not isolated from C_2 (the extremely high frequency-related phenomenon) and R_{dc}. The significance of C_2 in the C^* plane is that it is expected to be related to the lumped bulk behavior. At high frequencies, the charge carriers do not experience barrier, as they are driven and modulated by the ac small-signal amplitude over the electrical barriers. This can be portrayed as barrier 'shorting-out' as if they are transparent to electrical conduction in this frequency domain. Thus we obtain a lumped grain resistance effect at high measurement frequencies. This leads to an equivalent circuit element consisting of a capacitor and a resistor in parallel, $R_{dc} - C_2$ in Fig. 10c. Therefore, the duality between the two types of the equivalent circuit representation has a meaning and a demonstration is provided here as to how these elements respond to the situations and interpretations.

5. Conclusions

The multi-plane(Z^*, C^* and M^*) analytical approaches in a simultaneous fashion has been employed to elucidate the underlying operative mechanisms in a solid-state derived $CaSnO_3$ material system. Thus, the lumped parameter/complex plane analysis technique provided a meaningful solution to the underlying problem. Overall, the way ac electrical data have been handled, analyzed, and parameters extracted to understand their role within the microstructures, has been termed as immittance spectroscopy. Such in-depth investigation, involving multiple competing phenomena and operating mechanisms including the development of equivalent circuit model consisting of contributing and well-defined elements, is conducive to the understanding of the complexity of a material system.

Realistically, the dual representation of the equivalent circuit is a singly operative circuit across the sample (between the electrodes) depending on the interpreter's viewing approach. However, this dual representation converges to the single circuit when the underlying

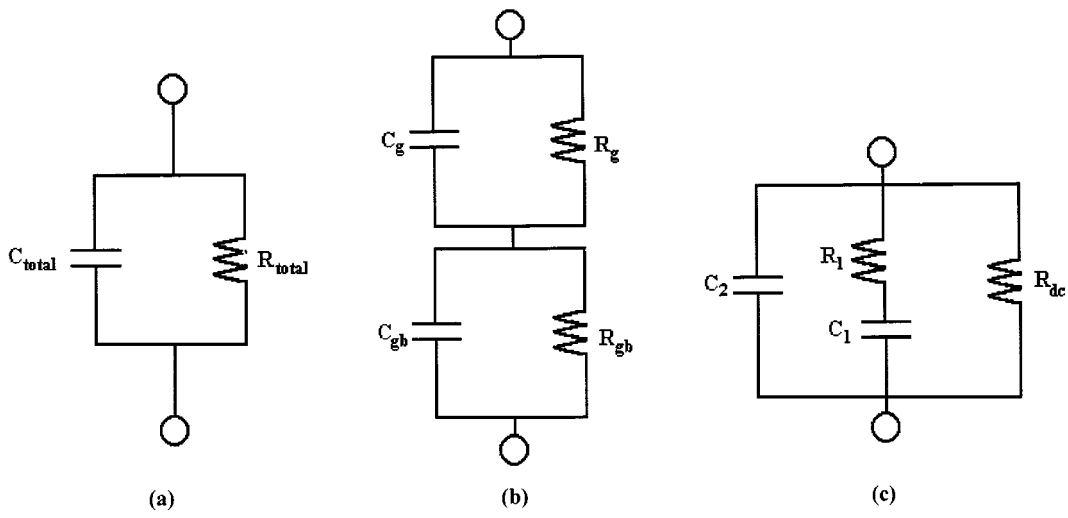

Figure 10 (a) Simple equivalent representation corresponding to the single-like lumped relaxation. (b) Equivalent circuit model corresponding to the elements extracted from the Z^*- and M^*-plane analyses. (c) Equivalent circuit model representing the C^*-plane behavior incorporating trapping response.

contributing elements are physically located and comprehended of their purpose as each circuit element.

This investigation reveals that $CaSnO_3$ can be used as capacitor material due to its invariance in the frequency domain possessing an ultra-small temperature coefficient of capacitance. The sintering temperature (1200–1350 °C) and soak-times (24–60 h) allowed to understand the processing conditions of the component preparation via the conventional reaction (SSR) kinetics. These kinetics assisted in determining the functional behavior of $CaSnO_3$ and its selectivity as a capacitor element. It is emphasized that densification plays a key role to the steady invariant capacitance and ultra-low TCC of this material.

The examination via Bode plots was used to support the analyses done by LP/CPA technique. The measurement frequencies (5 Hz–13 MHz) and elevated temperatures (25–300 °C) determined the variation/non-variation of the electrical paths between the opposite electrodes. The minute difference in the bulk dielectric behavior is attributed to the minor adjustment in the formation of the grain-to-grain contact region. The trapping parameters are believed to be less sensitive to the resulting dielectric as a capacitor element. This investigation indicated that downsizing in the scatter of the capacitance value is possible via small intervals in the soak-time at these sintering temperatures.

Acknowledgements

The authors wish to express their gratitude to Dr. Mansor Hashim for his generosity in allowing to use the HP4192A LF Impedance Analyzer on which the reported data were acquired. The assistance of the staff of electron microscopy unit at the Institute of Bioscience, UPM, is gratefully acknowledged. One of the authors (AMA) wishes to thank UPM for awarding a short-term grant to initiate research on $MSnO_3$ system.

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Received 3 September 1998
and accepted 29 January 1999